DESIGN AND CONTROL OF A BATTERY CHARGER FOR ELECTRIC VEHICLES

Adrià Marcos Pastor

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Design and Control of a Battery Charger for Electric Vehicles

Doctoral Thesis

Departament d'Enginyeria Electrònica, Elèctrica i Automàtica

Universitat Rovira i Virgili

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Supervised by Dr. Enric Vidal Idiarte

and Dr. Àngel Cid Pastor

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Tarragona, 2015

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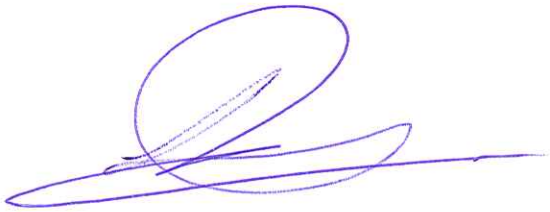
WE STATE that the present study, entitled "**Design and control of a battery charger for electric vehicles**", presented by Adrià Marcos Pastor for the award of the degree of Doctor, has been carried out under our supervision at the Department of Electronic, Electric and Automatic Control Engineering of this university.

Tarragona, 31th August 2015

Doctoral Thesis Supervisor

Dr. Enric Vidal Idiarte

Doctoral Thesis Supervisor



Dr. Àngel Cid Pastor

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Per a aquells que han estat,

els que som,

i els que han de venir.

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En primer lloc, voldria agrair als meus directors de tesis, el Dr. Enric Vidal Idiarte i el Dr. Àngel Cid Pastor, l'oportunitat que m'han donat de treballar en el desenvolupament d'aquesta tesi dins el Grup de recerca en Automàtica i Electrònica Industrial (GAEI) de la Universitat Rovira i Virgili. Els agraeixo profundament les hores que m'han dedicat i tot el suport que m'han donat al llarg d'aquest temps.

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List of abbreviations, symbols and variables

Abbreviations

AC	Alternating current
ADC	Analogue-to-digital converter
BCR	Battery current regulation
BMS	Battery management system
CC	Constant current
CCM	Continuous conduction mode
CPL	Constant power load
CPS	Constant power source
CV	Constant voltage
DB	Diode bridge
DC	Direct current
DPWM	Digital pulse width modulation
DSC	Digital signal controller
EMI	Electromagnetic interference
EV	Electric vehicle
EVSE	Electric vehicle supply equipment
G2V	Grid-to-vehicle
GPIO	General purpose input output
HEV	Hybrid electric vehicle
ICE	Internal combustion engine
IEC	International Electrotechnical Commission
LFR	Loss-free resistor
Li-ion	Lithium-ion
MOSFET	Metal–oxide–semiconductor field-effect transistor
NiMH	Nickel-metal hydride
OA	Operational amplifier
PF	Power factor
PFC	Power factor correction
PHEV	Plug-in hybrid electric vehicle
PI	Proportional-integral
POPI	Power output power input
PWM	Pulse width modulation
SAE	Society Automotive Engineers
SG	Smart grid
Si	Silicon
SiC	Silicon carbide
SM	Sliding-mode
SMC	Sliding-mode control
SoC	State of charge
THD	Total harmonic distortion
V2G	Vehicle-to-grid

Symbols and variables

α	Ratio between peak-line voltage and *RMS* DC-link voltage
A	Ampere, current unit
Δ	Increment or ripple
$\Delta i_{L,\ pk\text{-}pk}$	Peak-to-peak inductor current ripple

$\Delta v_{Bat,\ pk\text{-}pk}$	Peak-to-peak ripple of the battery voltage
$\Delta v_{C,\ pk\text{-}pk}$	Peak-to-peak ripple of the DC-link capacitor voltage
ΔZ_{dif}	Magnitude difference in dBs
C	Capacitor (also used as a subscript)
C_{Bat}	Battery capacitor
C_{in}	Input capacitor
cos	Cosine operation
d	Duty-cycle
D	Diode
F	Farad, capacitance unit
f_{AC}	Line frequency
f_C	Cut-off frequency
fs_2	DC-link regulation loop frequency execution rate
f_{SW}	Switching frequency
F_{RHC}	Ripple harmonic cancellation function
g	Emulated input conductance by each PFC stage cell
G	Emulated input conductance by the PFC stage
H	Henry, inductance unit
H	Hysteresis
i_{AC}	Line current
$I_{AC,RMS}$	*RMS* line current
$I_{AC,RMS\ max}$	Maximum *RMS* line current
$i_{Bat}(t)$	Instantaneous battery current
I_{Bat}	Average battery current
$i_{in}(t)$	Instantaneous rectified input current
I_{in}	Average input current
$i_{INT}(t)$	Instantaneous current sum of three interleaved inductor currents
$i_L(t)$	Instantaneous inductor current
I_L	Average inductor current
$i_o(t)$	Instantaneous output current from the PFC stage
I_o	Average output current from the PFC stage
k	Constant parameter
k_i	Integral parameter
k_p	Proportional parameter
L	Inductor (also used as a subscript)
m	Inductor current slopes
M	Type of current-mode controller
η	Efficiency
N	Number of cells
P	Average power
P_{Bat}	Average battery power
$P_{cell,max}$	Maximum rated power for one cell
P_{in}	Average input power
P_o	Average output power
$P_{o,\ max}$	Maximum load conditions
Q	MOSFET
Q_{rr}	Reverse recovery charge
r	Loss-free resistor emulated resistance
R	Resistor
RMS	Root mean square value (also used as a subscript)
s	Sliding-mode control surface
S	Siemens (Ω^{-1})
sin	Sine operation
t	Time
τ	ON-state conduction time

T	Loop gain
tan	Tangent operation
τ_{eq}	ON-state conduction time equivalent control
T_{S2}	DC-link regulation loop period execution rate
T_{SW}	Switching period
$u(t)$	Instantaneous control signal
$u_L(t)$	Instantaneous control signal for low-side controlled switches
$u_H(t)$	Instantaneous control signal for high-side controlled switches
V	Volt, voltage unit
$v_{AC}(t)$	Instantaneous line voltage
V_{AC}	Line voltage
$V_{AC,\,RMS}$	*RMS* line voltage
$v_{Bat}(t)$	Instantaneous battery voltage
V_{Bat}	Battery voltage
$v_C(t)$	Instantaneous DC-link capacitor voltage
V_C	Average DC-link capacitor voltage
$V_{C,\,RMS}$	*RMS* DC-link capacitor voltage
$v_{in}(t)$	Instantaneous rectified input voltage
V_{in}	Average rectified input voltage
V_M	Peak line voltage
W	Watt, power unit
W	Energy
ω_C	Cut-off angular frequency
ω_N	Discrete centre frequency of Notch filter
ω_o	Angular line frequency
Z	Impedance
Z_{in}	Input impedance
$Z_{o\text{-}CL}$	Closed-loop output impedance
$x(t)$	State vector
Ω	Ohm, resistance unit

Subscripts and superscripts

$_{Bat}$	Battery
$_{CL}$	Closed-loop
$_{conv}$	Conventional
$_{i}$	Relative to buck cells
$_{in}$	Input
$_{j}$	Relative to boost cells
$_{k}$	Any type of cell
$_{max}$	Maximum
$_{min}$	Minimum
$_{mod}$	Modulated
$_{n}$	n^{th} switching period
$_{o}$	Output
$_{pk}$	Peak
$_{ref}$	Reference
$_{Sel}$	Selected
$_{SS}$	Steady-state
^{T}	Transpose operation

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Abstract

This thesis presents the design and control of a battery charger for plug-in electric vehicles. The aim of this work is to demonstrate that it is possible to apply the discrete-time sliding-mode control theory to design discrete-time inductor current-mode controllers that can operate at a constant switching frequency. This hypothesis is validated in a 3 kW fully digitally controlled bidirectional battery charger that consists of a grid-synchronised rectifier followed by two-cascaded stages. The first stage is based on three interleaved boost converters connected in parallel while the second stage is composed by three interleaved buck converters connected to the battery. The whole digital control has been programmed in a single digital signal controller.

The proposed digital controller has been designed to impose a loss-free resistor behaviour on the first stage aiming to achieve a suitable power factor correction performance. The emulated input resistance of the first stage is adjusted by an outer loop that regulates the DC-link voltage value at 400 V_{DC}. Typical constant current and constant voltage operation modes in battery charging applications are also demonstrated for a battery current of 8 A and battery voltage of 380 V respectively.

On the other hand, two different DC-link voltage regulation strategies are proposed in this thesis to reduce the DC-link capacitance, which is generally present in many single-phase battery charging applications based on two-cascaded stages. This reduction aims to avoid the use of electrolytic capacitors owing to their low reliability with respect other technologies, such as polypropylene film capacitors. In particular, two different scenarios are analysed in detail. First one considers that the power factor correction stage regulates the DC-link voltage and the second stage behaves as a constant power load. In contrast, the second approach proposes a variable DC-link voltage reference tracking from the second stage, this allowing a further reduction of the DC-link capacitance.

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Chapter 1

INTRODUCTION

Electric vehicles (EVs) have emerged in the recent years as a feasible alternative to internal combustion engine (ICE) vehicles aiming to reduce the high petroleum's dependency and to comply with the more restrictive regulations on emissions that have derived from a major environmental concern about global warming [1, 2]. Despite the fact that the number of EVs is still far from being equal to conventional ICE vehicles, recent advances in energy storage technologies and electronics engineering are boosting their growth in the automotive sector. Although this technology seems to be relatively new, the first EV was invented in 1834 and during the 19th century it was produced and commercialised by some American, British and French companies [3, 4]. However, EVs were not considered as a competitive solution to personal road transportation at that time because of the fast advancement of ICE vehicles together with the front barriers associated with the batteries.

Nowadays, some automakers are promoting hybrid electric vehicles (HEV) to tackle the disadvantages of conventional ICE vehicles and pure electric vehicles at once since a fast direct transition to pure electric vehicles is not possible. The architectures of HEVs can be series, parallel, series-parallel or complex [4]. Their control algorithms play an important role because the key point of HEVs is to optimise the driving efficiency through the operation of both ICE and electric motor drive(s) depending on the conditions. Even though these vehicles can generate very low emissions, they cannot be considered completely emissions-free vehicles. Moreover, the need for additional motors, electric storage systems and power converters results in a cost increase of the overall system. According to the adopted terminology, those HEVs that can be charged by being plugged to the grid receive the name of plug-in hybrid electric vehicles (PHEVs).

On the other hand, different companies are betting for full EVs stimulated by the last advancements in energy storage technologies and power electronics. For instance, Tesla Motors has recently presented Model S which is capable to cover a distance of 430 km with a full charge of the battery [5]. However, despite their main advantages, such as high energy efficiency, independence on fossil fuels and zero emissions, the main drawbacks of EVs are their high initial cost, relative short driving autonomy, life cycle of the batteries and slow

charging. In order to simplify the notation, both PHEVs and pure EVs will be referred as EVs hereinafter.

Regarding the employed battery technology in EVs, the nickel-metal hydride (NiMH) batteries were the most widely used energy storage technology during the 1990s and 2000s due to their high power density and proven safety [6-8]. These days, lithium-ion (Li-ion) batteries are considered the most promising battery technology for EVs as a result of its relatively higher specific energy and power density with respect to lead acid and NiMH. A higher specific energy density is generally traduced into higher autonomy, which is a highly appreciated characteristic in the automotive sector. However, Li-ion batteries need to use a more complex battery management system (BMS) to provide different protections, such as overvoltage, undervoltage, overtemperature and overcurrent; in addition to voltage cell's equalisation [6, 8].

Despite the clear benefits of using EVs, other challenges have still to be faced on the way to electro mobility, such as the lack of charging infrastructure for a deep penetration of EVs in the electric power systems that currently exist. It is clear that EVs represent a new load on the distribution networks and a rapid increase in the number of these vehicles could eventually overload the power grid in case of an unexpected peak of energy consumption [9-12]. This issue gives an excellent opportunity to the concept of smart grids (SGs) to cope with a more efficient management of the electric energy through the distribution networks. In this sense, different approaches have been developed to coordinate the charging of EVs in order to minimise the distribution losses and voltage deviations [13,14]. The implementation of advanced metering infrastructures [9] and safe communication protocols to correctly manage the distribution network and its data is fundamental to make SGs a reality [15, 16].

Furthermore, load shifting has also motivated the research on how EVs connected to the grid can help in load balancing. Unbalanced load conditions between power generation and power consumption are partially generated due to the intrinsic variability of energy generation from renewable energy sources which only produce energy when the primary resource is available. A large number of EVs connected to the grid can be a potential solution to absorb the renewable energy that is not required in the moment that it is being generated [17], hence avoiding its loss [10]. Moreover, the vehicle-to-grid (V2G) capability [18], which enables EVs to inject energy into the grid, can also contribute in stabilizing unbalanced situations during peak hours or even provide electric energy for emergency backup during a power outage [19, 20]. Hence, it can be assured that the bidirectional power flow capability of EVs connected to SGs stands as one key opportunity that electro mobility is offering us to distribute more efficiently both generated and consumed electric energy [21].

1.1 Battery charging modes for EVs

International organizations, such as the International Electrotechnical Commission (IEC) and the Society of Automotive Engineers (SAE), are making an important effort in the development of different standards which regulate the connection of EVs to the power grids. Some of the most important standards are:

- IEC 61851-1 [22]. This standard defines the charging levels and refers to the characteristics and operating conditions of the supply device and the connection to the vehicle.
- IEC 62196-1 [23]. It mainly defines plugs, socket-outlets, vehicle connectors and inlets for EV/PHEVs.
- IEC 61980-1 [24]. It is applied to the equipment for the wireless power transfer from the supply network to electric road vehicles.
- SAE J1772 [25]. It covers the general requirements to facilitate conductive charging of EV/PHEVs in North America.

Four different EV charging modes are defined in [22]. A residual current device is required for all charging modes.

- Mode 1. It is the most basic charging mode. It can be employed in single-phase or three-phase power systems of maximum 250 V_{RMS} and 480 V_{RMS} respectively. The maximum allowed *RMS* current is 16 A and no specific connector for the EV is required. This mode is not allowed in United States (US).
- Mode 2. It can be employed in single-phase or three-phase power systems of maximum 250 V_{RMS} and 480 V_{RMS} respectively. The maximum allowed *RMS* current is 32 A and no specific connector for the EV is required. It requires an inline control box.
- Mode 3. The EV is connected to the power grid by means of a specific electric vehicle supply equipment (EVSE) and the inline control box is extended to the employed EVSE. The connection can be single-phase or three-phase and the rated maximum *RMS* current ranges from 32 A to 250 A.
- Mode 4. The EV is connected to the power grid by means of an off-board battery charger through a DC connection. The maximum rated current is 400 A.

Both modes 1 and 2 are considered slow charging modes and they are expected to take place in residential areas through common household outlets overnight and allow reaching battery full capacity before morning [26]. Charging mode 3 is considered a semi-slow charging mode and, although it can be implemented in most of the environments, it is likely to be installed in

parking lots, shopping-centres, hotels, etc., for client service [27]. Finally, mode 4 is meant to allow a full recharge of the batteries in few minutes and it is likely to be used in roads and rest areas of highways [26].

1.2 EVs battery chargers

Several battery chargers can be found in the literature and they can be classified according to different criteria [28]. A first classification deals with the battery charger location, which can be inside or outside of the vehicle. Those battery chargers that are placed inside of the vehicle are called *on-board* battery chargers whereas the *off-board* battery chargers are placed outside. On-board battery chargers are more power limited because of their weight and volume constrains, so that they can be used for battery charging modes 1 and 2 [27]. In some cases, on-board battery chargers are integrated with the electric drive of the vehicle in order to avoid adding extra inductors and switches which would only be employed for charging the battery [29-31]. In contrast, off-board battery chargers are mainly designed for battery charging modes 3 and 4 since they are not subjected to weight and size limitations.

Battery chargers can also be classified into conductive and inductive. Conductive battery chargers are defined as those charging systems that use a direct physical contact between the connector and the charge inlet [22]. On the contrary, inductive chargers are those that transfer the power magnetically. Although some works deal with moving chargers [32], inductive chargers are mainly considered for stationary slow charging applications [33].

Another feature that can be used to classify the battery chargers is galvanic isolation. While isolation is recommended for safety reasons, it generally results in heavier and bigger structures which require the use of more complex controllers.

Finally, the bidirectional capability of battery chargers to absorb energy or to inject back to the grid contrasts with unidirectional battery chargers which are only meant to charge the battery. As it can be deduced, bidirectional battery chargers consist in a more expensive, heavier and bigger solution than unidirectional chargers because they generally need extra circuitry to operate in both directions of the power flow.

1.3 EVs battery chargers architectures

Most of on-board single-phase battery chargers consist of two cascaded stages [28] (see Fig. 1.1). First stage consists of an AC/DC converter that ensures a unity power factor correction (PFC) by absorbing a sinusoidal current from the grid with low current harmonics in order to comply with standard IEC 61000-3-2 [34]. Second stage is based on a DC/DC converter which regulates the current that is delivered to the battery according to its state of charge (SoC) and

matches the difference between the DC-link and battery voltages. Both stages are generally connected by means of a DC-link capacitor. An electromagnetic interference (EMI) filter is connected between the grid and the first stage to comply with standard CISPR 22 [35].

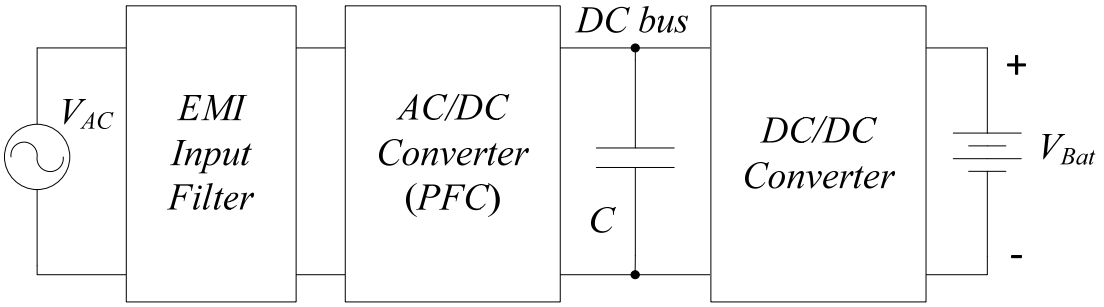


Fig. 1.1. General block diagram of a single-phase on-board battery charger.

1.3.1 PFC stage circuit topologies

A diode rectifier followed by a boost converter is the most popular unidirectional AC/DC converter owing to its continuous input current, simple structure and grounded transistor [36-38] (see Fig. 1.2.a). However, the main drawback is that an important share of conduction losses is generated by the diode rectifier. For this reason, several bridgeless topologies have been proposed to avoid the use of a rectifier, so that a higher efficiency can be achieved [39-42] (see Fig. 1.2.b-d).

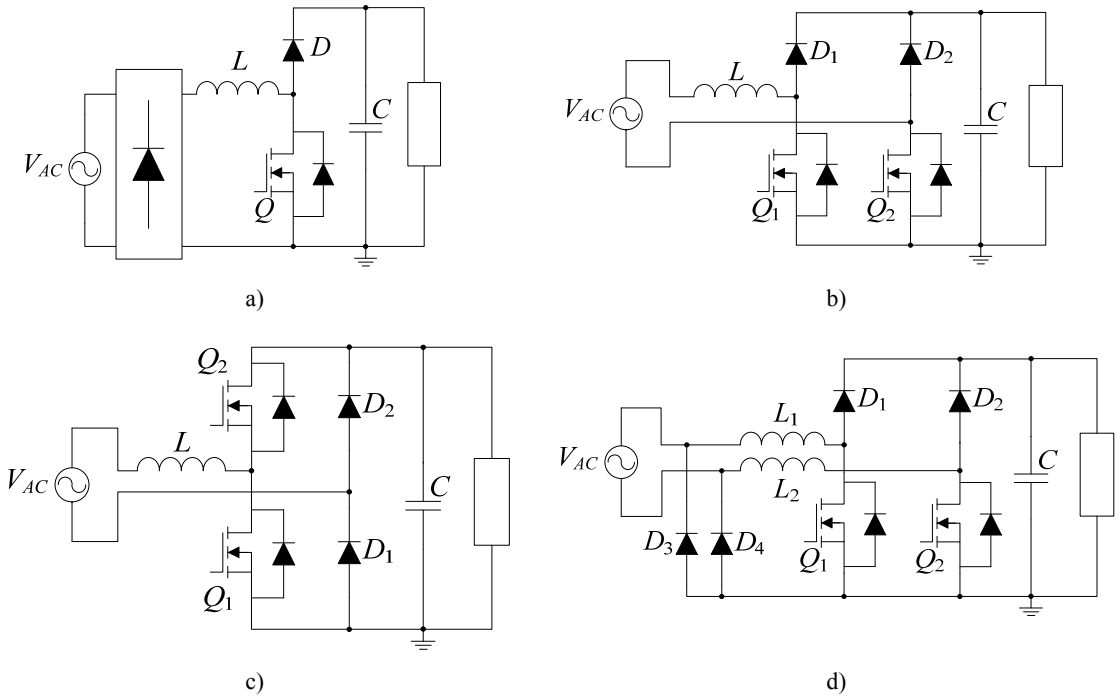
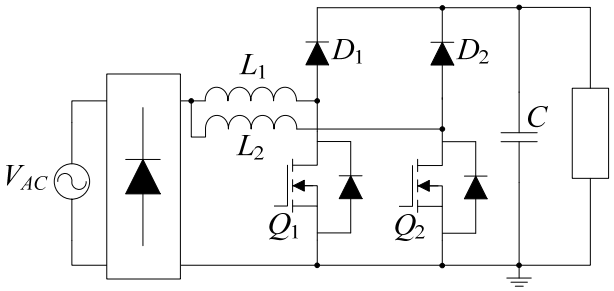


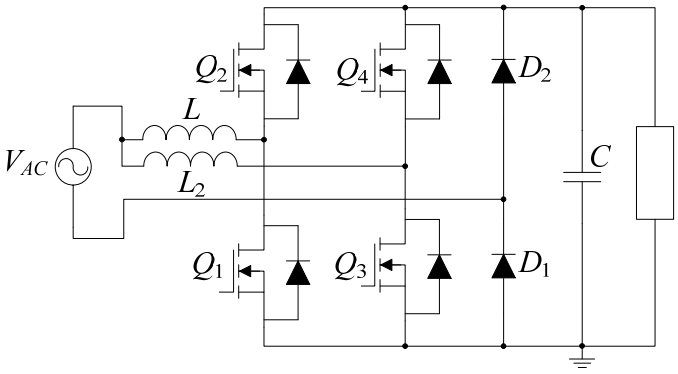
Fig. 1.2. Unidirectional boost-based AC/DC converters. a) Diode rectifier and boost converter. Bridgeless topologies b) Basic topology [39]. c) Totem-pole [40]. d) Dual-boost or semi-bridgeless [41].

The connection of different converters in parallel is considered a suitable strategy to deal with higher power levels without increasing the current stress of the components (see Fig. 1.3.a). Besides, the interleaving operation of parallel-connected converters was intended to reduce the size of filtering components and the current ripple stress at which input and output capacitors are subjected to [43-45]. This technique can be also extended to bridgeless topologies [46, 47] as can be observed in Fig. 1.3.b-c.

a)



b)



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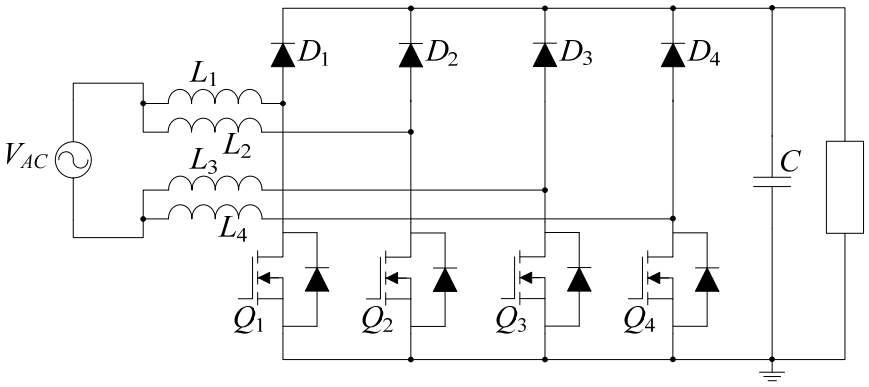


Fig. 1.3. Unidirectional interleaved boost-based AC/DC converters. a) Basic interleaved [43, 44]. b) Totem-pole interleaved [47]. c) Bridgeless interleaved [46].

The diode rectifier of a unidirectional boost converter can be substituted by a synchronous rectifier to allow the bidirectional power flow capability (see Fig. 1.4.a). However, a better efficiency can be achieved if one leg of the synchronous rectifier is replaced by the bidirectional

boost converter (see Fig. 1.4.b). Furthermore, it is also possible to apply the interleaving technique as illustrated in Fig. 1.4.c.

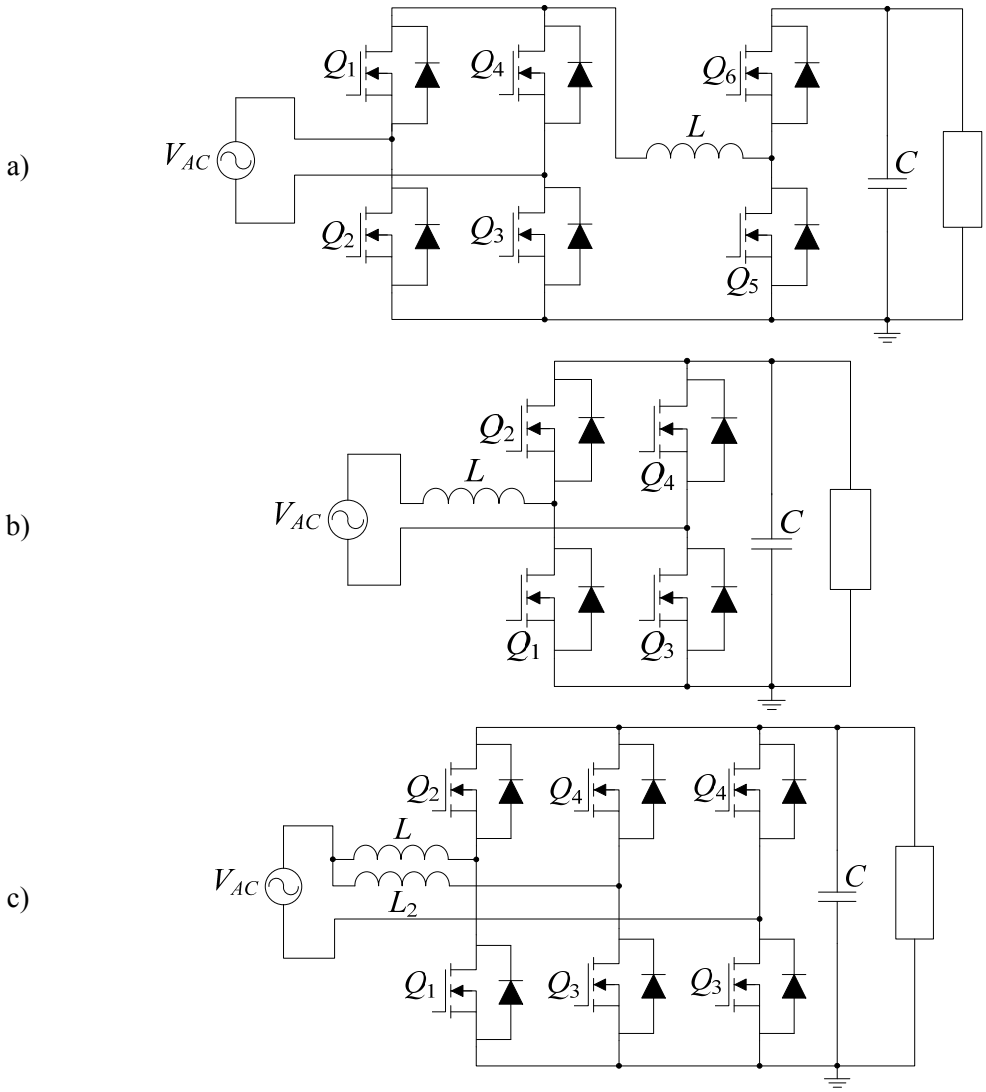


Fig. 1.4. Bidirectional boost-based AC/DC converters. a) Boost converter with synchronous rectifier. b) Full-bridge boost rectifier [48]. c) Full-bridge interleaved [48, 49].

1.3.2 Battery current regulation stage circuit topologies

The voltage of many batteries for EVs ranges from 100 V to 400 V and, for that reason, the most employed DC/DC converter for the battery current regulation (BCR) stage consists of a unidirectional buck converter in order to reduce the voltage from the DC-link to the voltage level of the battery (see Fig. 1.5.a) Sometimes an LC output filter is added to reduce the filtering components (see Fig. 1.5.b). Unidirectional buck-boost converters are also considered due to their capability to step-up and step-down the output voltage (see Fig. 1.5.c). In addition, interleaving technique can be applied on these topologies [50, 51] as depicted in Fig. 1.5.d-e. In particular, a diode rectifier followed by two interleaved buck-boost converters is proposed in [51] to design a single-stage battery charger.

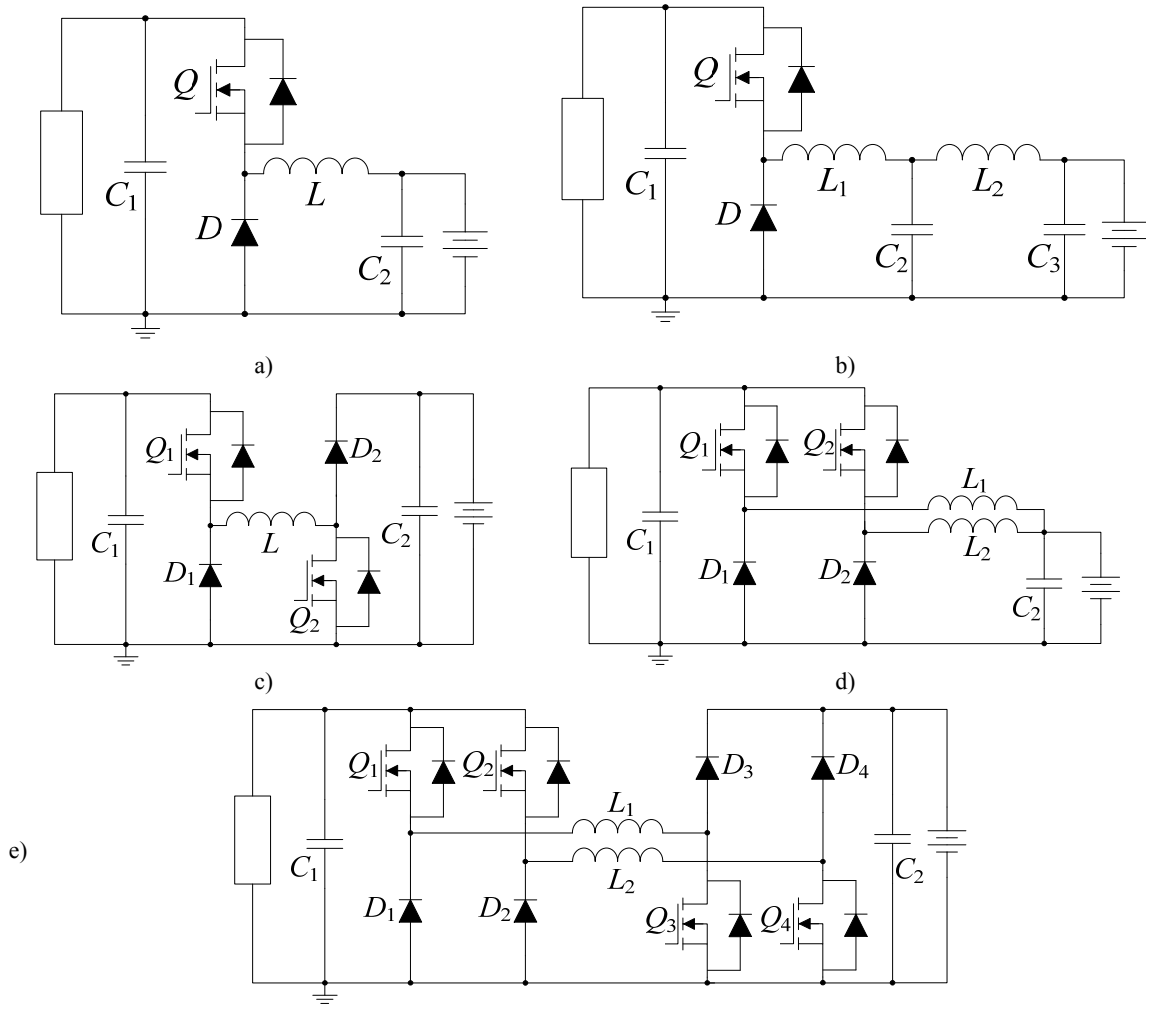


Fig. 1.5. Unidirectional non-isolated DC/DC converters. a) Buck. b) Buck with output filter. c) Buck-boost. d) Interleaved buck [50]. e) Interleaved buck-boost [51].

Other topologies include a high-frequency switched transformer to provide galvanic isolation between the grid and the battery [27]. In this sense, it is preferable to use high-frequency switched transformers in terms of size and weight than line-frequency transformers [52]. Two of the most widely used topologies are the phase-shifted full-bridge DC/DC converter [53] and the full-bridge series resonant converter [54] (see Fig. 1.6).

Regarding bidirectional topologies, it is very common to find in the literature the use of a two quadrant buck converters (or bidirectional buck converters) since it can be also used for the traction power system to supply energy to the DC-link that feeds the inverters that are used for controlling the electrical drive of the vehicle [55, 56] (see Fig. 1.7.a). Bidirectional topologies for buck-boost [55] and interleaved buck [26, 27, 58] are also proposed in the literature and are depicted in Fig. 1.7.c-d respectively.

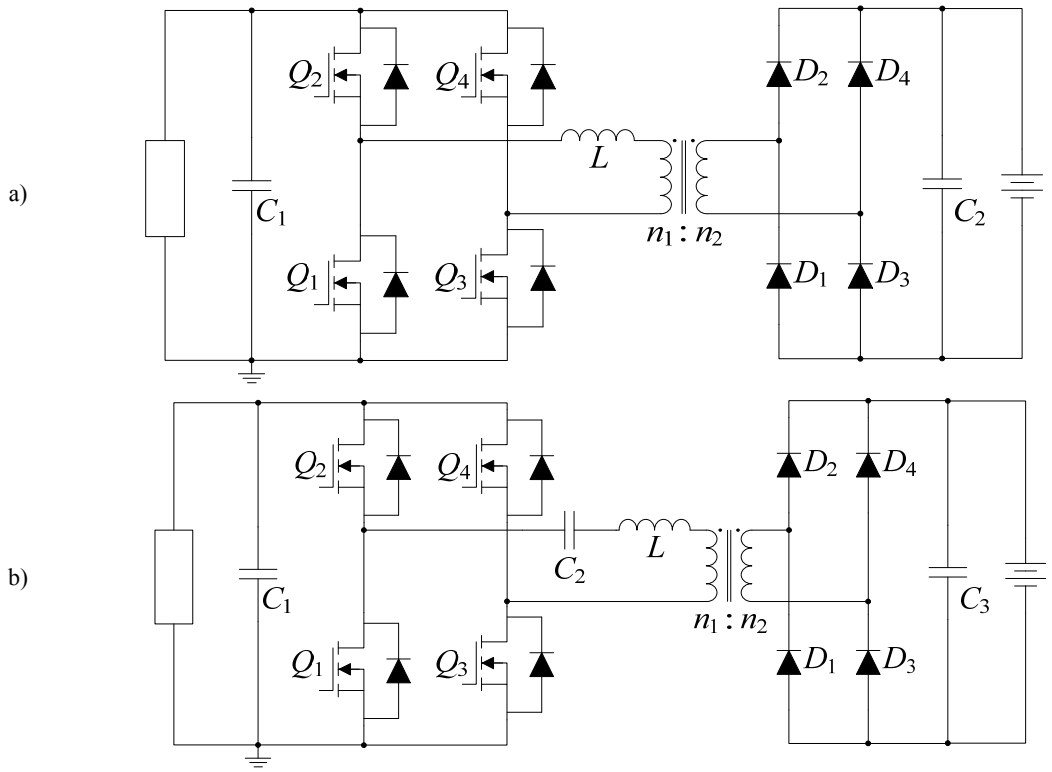


Fig. 1.6. Unidirectional isolated DC/DC converters. a) Phase-shifted full-bridge [53]. b) Full-bridge series resonant [54].

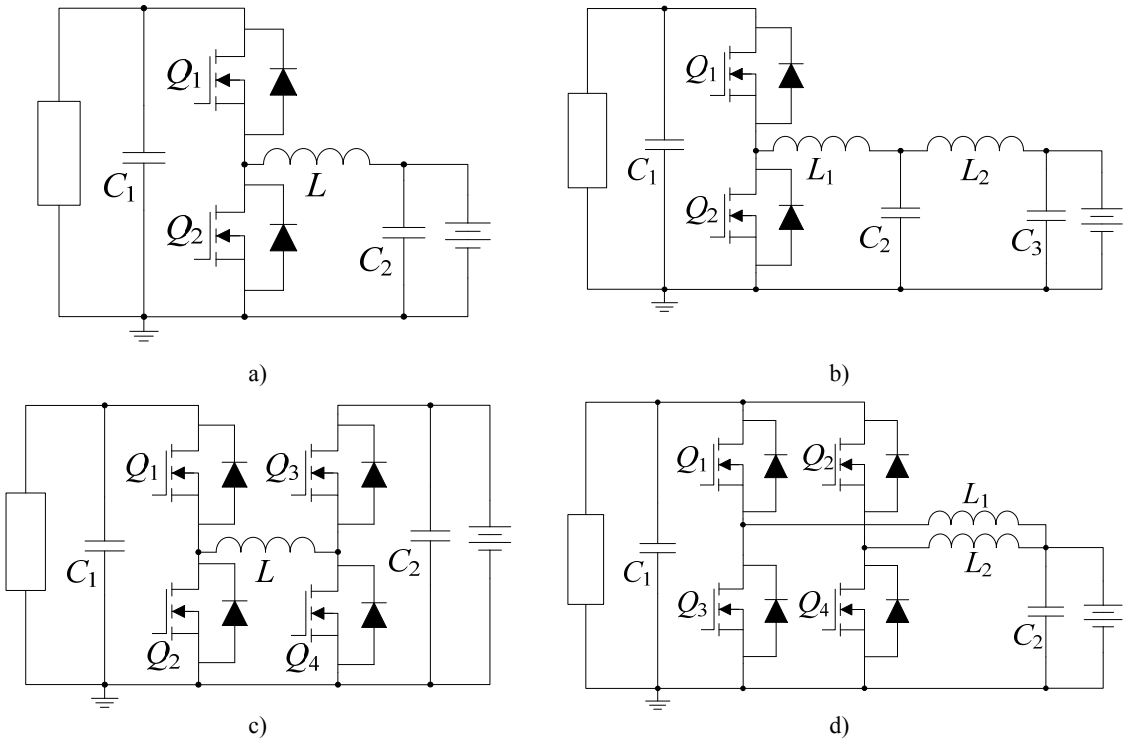


Fig. 1.7. Bidirectional non-isolated DC/DC converters. a) Two quadrant buck [55]. b) Two quadrant buck with output filter [59]. c) Buck-boost [55]. d) Interleaved two quadrant buck [58].

Moreover, dual-active bridge [53, 60], bidirectional full-bridge series resonant [61] converters and derived-topologies are also employed in EV battery charging applications to provide battery chargers with galvanic isolation and bidirectional power flow capability.

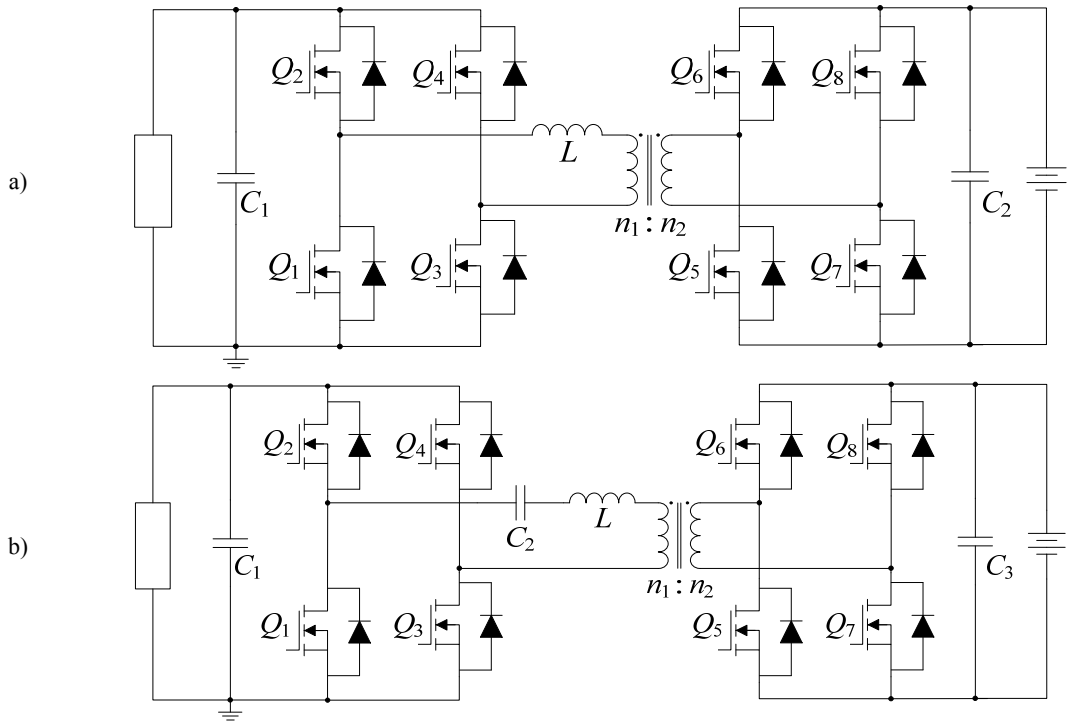


Fig. 1.8. Bidirectional isolated DC/DC converters. a) Dual-active bridge [53]. b) Full-bridge series resonant [61].

1.4 Battery charger controllers

The most common strategy to design the controllers of two-stage-based battery chargers is to design one controller for each stage (see Fig. 1.9). On one hand, the PFC controller ensures the proportionality between the input voltage and the input current, this achieving a unity power factor (PF). In addition, the PFC controller is generally responsible of regulating the DC-link voltage at the specified voltage reference. On the other hand, the BCR stage delivers the required current to the battery depending on its SoC.

The classical strategy for single-phase PFC controllers consists of an inner loop that controls the input current while an outer loop regulates the DC-link voltage [62]. The reference of the inner loop is obtained by multiplying the output of the outer loop with the sensed input voltage. Some approaches use a phase lock loop system to avoid sensing the grid voltage under polluted conditions [63]. The bandwidth of the outer loop has to be sufficiently low (10 Hz – 20 Hz) to reduce the injection of low-frequency harmonics into the grid current. Sometimes, notch filters are introduced into the outer loop to eliminate oscillations at twice the line frequency from the output of DC-link voltage compensator [64], therefore, voltage regulators can be provided with higher bandwidth [65].

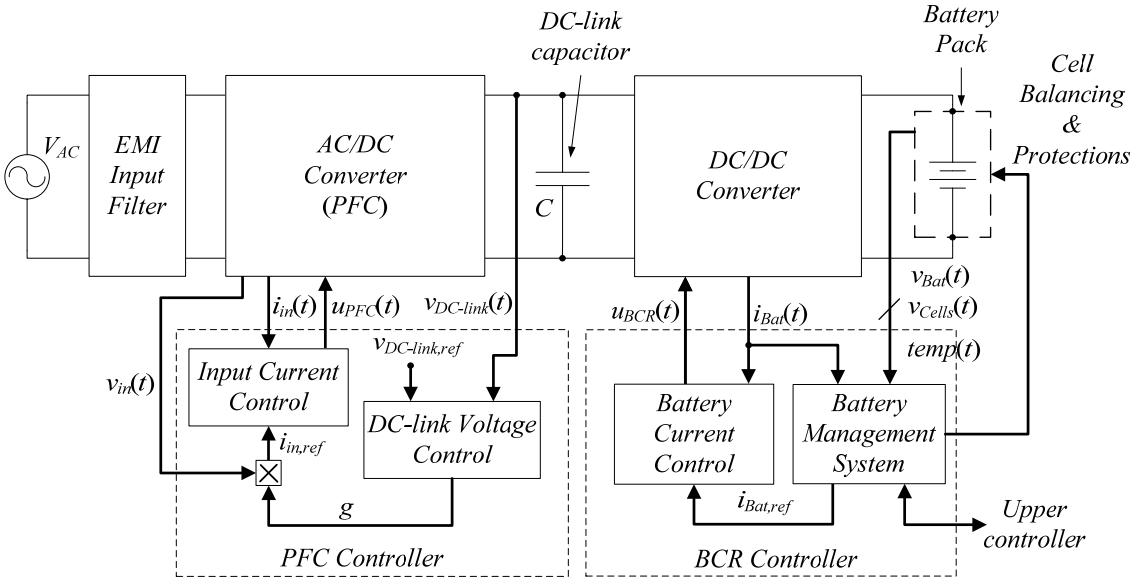


Fig. 1.9. Block diagram of a generic battery charger controllers.

Besides, BCR controllers consist of an inner loop that regulates the battery current according to the battery current reference that is generated by the BMS. Battery current reference is calculated depending on the SoC of the battery, which is estimated depending on different parameters such as battery voltage, temperature, etc. The BMS is also responsible of balancing the cells that configure the battery pack as well as activing any protections if necessary. The BMS can be eventually communicated with an upper controller [8].

The most popular procedure to charge a battery is the constant current constant voltage method (CC-CV) [66, 67]. The battery is first charged with a constant current (CC) until the battery voltage reaches a predetermined value. In that moment, the operation of the battery charger switches into constant voltage (CV) mode during which the battery current is decreased progressively along with the SoC of the battery (see Fig. 1.10). However, the advancements in microprocessor control units motivated the development of other strategies with higher levels of computational requirements [68]. Some examples are the genetic algorithm in [68] that determines the optimal charging current according to a predictive model of the battery, the fuzzy controller in [69] or the optimal sinusoidal battery current proposed in [70]. The latter approach proposes the frequency and amplitude modulation of a sinusoidal current that is introduced to the battery in order to find the lowest input impedance behaviour of the battery, so that the charging operation is more efficient.

During the last decade, the application of digital controllers has also been extended to the field of power electronics motivated by their cost and size decrease as well as the increase in their computation capability [71]. In the particular case of battery charging applications for EVs, digital controllers are specially preferred instead of analogue controllers due to the high

complexity and cost that would imply the corresponding analogue implementation for the whole system's management. However, the high sampling frequency and the implementation of the control algorithms for the PFC and BCR stages by means of only one digital controller is not obvious. For that reason, some two-stage battery charger manufacturers use two digital controllers or a mixed combination of both analogue and digital controllers to design their solutions [50].

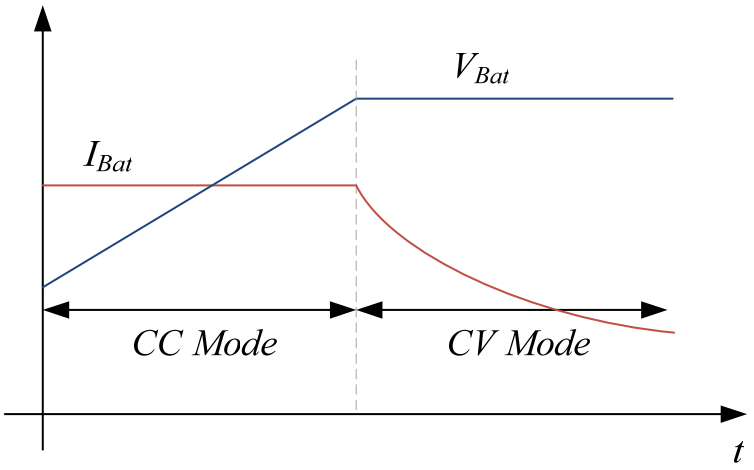


Fig. 1.10. CC-CV battery charging profile.

Regarding the design of current-mode controllers, a large number of different inductor current-mode controllers have been proposed in the literature [72, 73] which, roughly speaking, can be classified into two categories, constant and variable switching frequency-based controllers. Hysteretic current-mode control technique is one of the most employed type of variable switching frequency-based current-mode controller and its use goes back in time to the early years of DC-DC switching converters when the resulting regulators were called self-oscillating [74]. This is because the change of topology is produced by the change of the internal state of the converter rather than by the action of an external signal as happens in pulse-width modulation-based (PWM) systems [73]. It has been shown recently that the most appropriate technique to describe the dynamic behaviour of hysteresis-based switching converters is sliding-mode control (SMC) approach [75] provided that sliding motions can be induced in the variable structure system describing the switching converter [76]. Moreover, the use of SMC has allowed the synthesis of loss-free resistors (LFRs) [77] by establishing the requirements that power converters must fulfil in order to present a proportional relation between both input voltage and current in sliding regime. An LFR consists in a two-port structure whose input current is proportional to the input voltage and all the absorbed input power P_{in} is ideally

transmitted to the output port. For that reason, LFRs are modelled as in Fig. 1.11 and are considered a type of POPI (Power Output=Power Input) systems, because it is supposed that there is no power loss during the power transmission. This kind of behaviour is of special interest in PFC and impedance matching application [78-82].

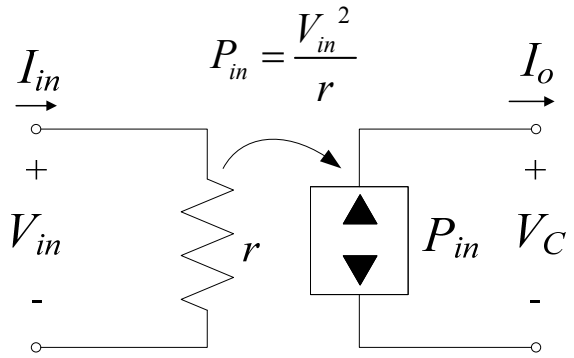


Fig. 1.11. Loss-free resistor (LFR) model.

However, despite hysteretic current-mode controllers exhibit a high performance in terms of robustness, stability and fast dynamic response [83-87] (see Fig. 1.12), they are not the most suitable solution for AC-DC power conversion applications. The reason is that its variable switching frequency complicates the design of filtering elements and the application of interleaving technique is limited to specific configurations [88, 89]. Hence, constant-frequency-based current controllers are more attractive in PFC applications [90-94] and, for that reason, a number of studies have proposed sliding-mode-based implementations with constant switching frequency [95-98] to provide a fast dynamic response similar to that exhibited by hysteretic-based sliding-mode (SM) controllers. In [98], the correspondence between the equivalent control in SM and the zero-dynamics non-linear PWM control is applied to a boost converter behaving like an LFR. However, the drawback of this controller is that it needs an analogue divider, which is a bulky component that is difficult to adjust and can be saturated for a zero value of the denominator. This fact suggests that the task of designing constant switching frequency SM-based current controllers should be carried out from a discrete-time point of view to make its further implementation easier. In addition, the use of a constant switching frequency permits a direct application of the interleaving technique.

Hence, this work proposes the application of the discrete-time SMC theory [76] to obtain a design methodology for competitive current controllers that operate at a constant switching frequency (see Fig. 1.13). However, since valley (and peak) current-mode controllers tend to introduce a high distortion on the third harmonic of the input current in PFC applications [99], the design of average current-mode controllers is also proposed. Furthermore, the DC-link

voltage regulator can be designed from the resulting discrete-time small signal model of the ideal sliding dynamics of the inner loop.

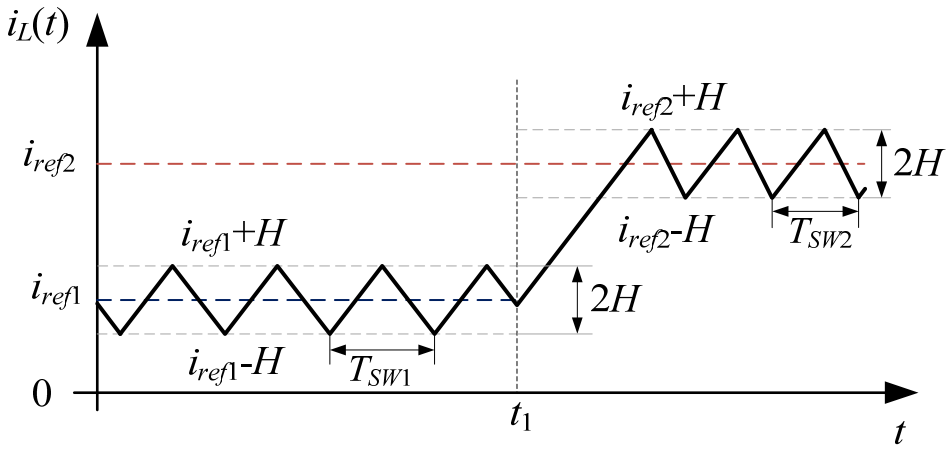


Fig. 1.12. Response of an inductor current in front of a reference step change in case of using a hysteretic current controller. T_{SW1} and T_{SW2} are the switching periods for the equilibrium points corresponding to i_{ref1} and i_{ref2} respectively and H represents the value of a hysteresis bound.

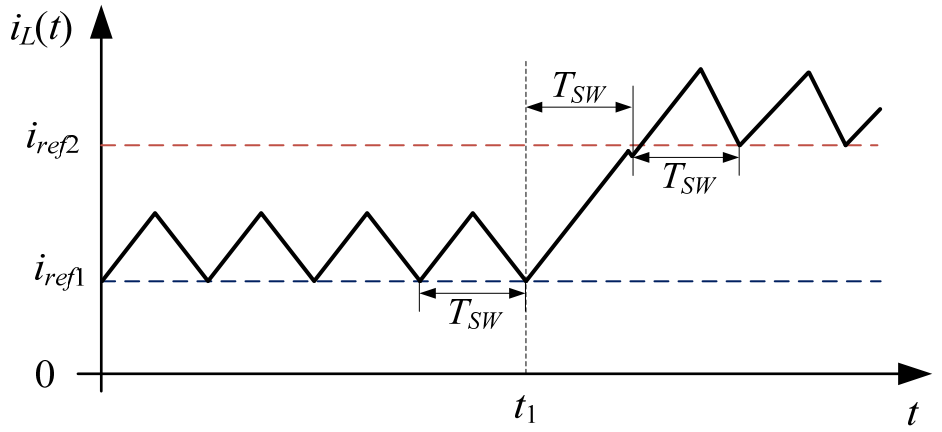


Fig. 1.13. Response of an inductor current in front of a reference step change in case of using the proposed controller. T_{SW} is the constant switching period.

As will be seen, the application of discrete-time SMC control theory requires the use of the internal model of the converter, so that, the proposed strategy is expected to result in a predictive model current-mode controller [100, 101]. A widely used family of constant switching frequency predictive current controllers is presented in [102], including valley, peak and average current-mode controllers for the three basic power converters (i.e. boost, buck and buck-boost). These predictive controllers calculate the duty cycle of the next switching period using the parameters of the plant, the present duty cycle and the samples of inductor current, input and output voltages. Other strategies use two samples of the inductor current two calculate the required duty cycle of the present switching period by means of a predictive interpolation technique [103]. It has been demonstrated in [104] that boost converters working as pre-

regulators and managed by predictive current-mode controllers can achieve a better quality of input current waveform than, for example, discrete-time proportional-integral (PI) current-mode controllers because their dynamic response is faster.

1.5 Research objectives and methodology

As it has been observed, most of plug-in battery chargers are based on two-cascaded stages, one for pre-regulation purposes and another one for matching the voltage difference between the DC-link and the battery. Besides, although the use of digital controllers in battery charging applications has increased in the recent years due to its flexibility and capability to integrate complex algorithms, they are mainly employed for slow tasks such as battery SoC monitoring and communication with other systems. In contrast, analogue or hybrid controllers (combination of analogue and digital control circuits) are preferred to regulate variables with faster dynamics, such as inductor currents and capacitor voltages.

The objective of this thesis is to apply the discrete-time SMC theory [76] to design constant-frequency-based inductor current-mode digital controllers with fast dynamic response. The designed controllers will be employed in a fully digitally controlled 3 kW battery charger for EVs (see Fig. 1.14). The selected battery charger topology will be based on two-cascaded stages which will be configured by three interleaved converters. In addition, the battery charger will be designed not only to absorb power from the grid, but also to allow its injection back if required.

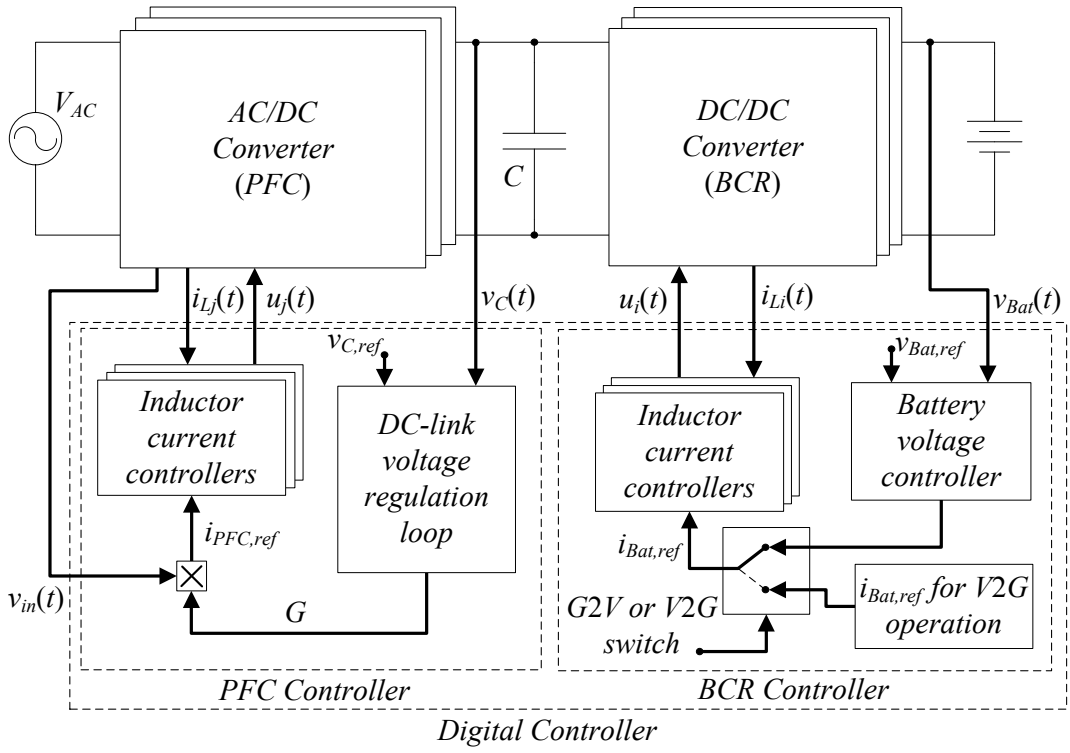


Fig. 1.14. Simplified block diagram of the battery charger control algorithm.

One implementation requirement is to design a control algorithm to be programmed in a single TMS320F28335 digital signal controller (DSC) from TEXAS INSTRUMENTS. On one hand, the PFC controller will have to impose an LFR behaviour on the first stage to achieve a unity PF. Moreover, the PFC controller will have to regulate the DC-link voltage at the desired voltage. On the other hand, the BCR controller will have to ensure a proper battery current regulation according to the battery voltage. Therefore, the control algorithm should include six discrete-time SM-based inductor current-mode controllers, the DC-link voltage regulation loop and the battery voltage controller (see Fig. 1.14).

Besides, an additional objective of this thesis is to reduce the DC-link capacitance that is generally present in most of two-stage-based battery chargers. For that purpose, several strategies based on the DC-link voltage controller design will be analysed in detail. The conventional design of the DC-link capacitors usually results in a high capacitance which is traditionally achieved by means of electrolytic capacitors due to their high power density. However, these capacitors exhibit shorter lifespan and higher series resistance with respect other technologies, such as polypropylene film capacitors. Thus, automotive industry is working toward the reduction of the DC-link capacitance in order to avoid the use of electrolytic capacitors in DC buses and, in consequence, be able to produce more reliable and longer lifespan battery chargers. In this sense, two different scenarios will be studied to achieve an important reduction of the DC-link capacitance. The first one focuses on the employed inductor current-mode controller in the PFC stage for the general system's operation, i.e., the PFC stage is responsible of regulating the DC-link voltage while the second stage of the battery charger behaves as a constant power sink. In contrast, the second scenario considers that the DC-link voltage is regulated by the second stage of the battery charger while the first stage only has to ensure a correct PFC performance.

Hence, the first four chapters of this thesis correspond to the design of the battery charger prototype and the digital controller. Before designing the control algorithm, it is necessary to obtain a discrete-time model of the system to be used in the design of the discrete-time SM-based current-mode controllers and PI voltage controllers. Simulation and experimental results are provided afterwards in Chapter 5. Finally, Chapter 6 corresponds to the DC-link capacitance reduction analysis which also includes simulation and experimental results.

Chapter 2

BATTERY CHARGER CIRCUIT DESIGN

This chapter describes how the bidirectional battery charger circuit has been designed and specifies the components that have been selected for its implementation. The chapter starts with a description of the proposed topology and the specifications that have been considered in the design process of the battery charger. Special attention has been paid to the interleaving operation of the different converters in order to study the resulting ripple harmonic cancellation effect on input and output currents. The chapter continues with the design of both power stages and the grid-synchronised rectifier. It also includes detailed information about the employed sensing circuitry and how analogue sensing signals have been properly conditioned to be sampled by the digital controller. Finally, it explains how the different drivers of controlled switches receive the corresponding control signals depending on the direction of the power flow.

2.1 Battery charger overview

2.1.1 Proposed topology

The proposed topology of the battery charger can be observed in Fig. 2.1. It consists of a full-bridge grid-synchronised rectifier which is connected to two-cascaded stages. Each stage is composed of three parallel converters in order to reduce the current stress of their power components. In addition, the interleaving technique has been applied aiming to take advantage of the ripple cancelation effect which is expected to entail a direct improvement on the performance of the PFC stage which is composed by three bidirectional boost converters that share the same DC-link capacitor. This stage is meant to pre-regulate the voltage of the DC-link capacitor without distorting the grid current in order to achieve a unity power factor. In contrast, the second stage is configured by three bidirectional buck converters which are directly tied to the battery and are responsible for supplying the required DC current to the battery depending on its SoC. For that reason, it has received the name of the BCR stage. Therefore, it is possible to summarise the main characteristics of the proposed battery charger topology as: single-phase, non-isolated, two-cascaded stage-based and bidirectional.

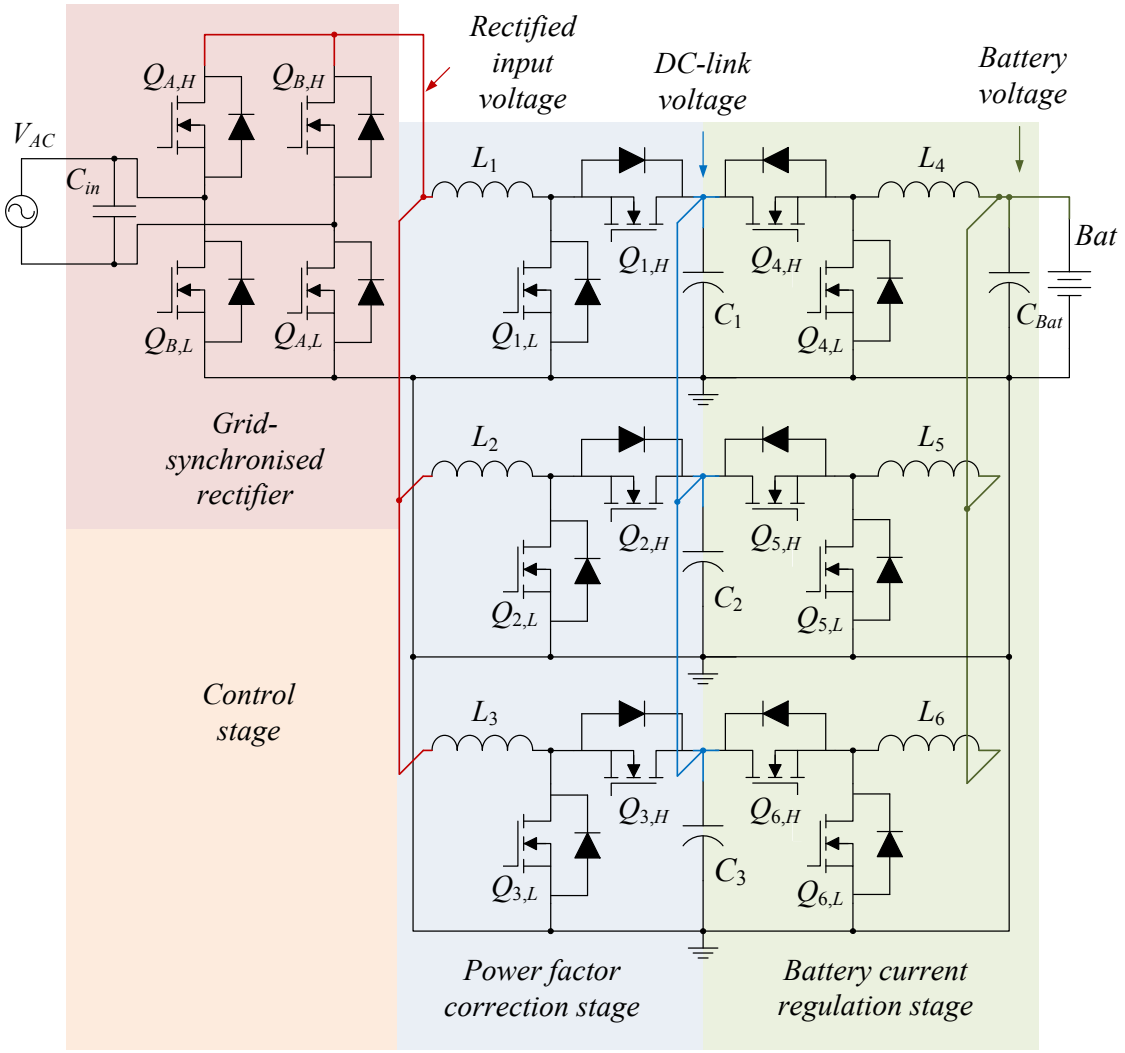


Fig. 2.1. Proposed battery charger topology.

2.1.2 Design Specifications

The design specifications of the battery charger can be found in Table 2.1. These specifications are common in the field of EV battery charging applications.

The full-bridge synchronous rectifier has been designed to handle the maximum total power because the whole current of the PFC stage is flowing through it. However, all converters have been designed to hold a third of the maximum total power, meaning that each cell has been designed for a rated power $P_{cell,\ max}$ of 1 kW. Hard-switching operation has been selected for its simplicity although it is less efficient.

Finally, it is worth commenting that, although the previous specifications consider universal line characteristics, only high line voltage conditions will be considered to simplify the design process. It is worth noting that it is not possible to design a battery charger for low line voltage conditions for a rated power of 3 kW because i_{AC} current is limited to 16 A_{rms}. In consequence,

the maximum achievable power under low line voltage conditions would be 1.8 kW approximately. Moreover, high line voltage conditions imply a higher voltage variation of the rectified input voltage, which arise more restrictive design considerations.

Parameter	Symbol	Specified Value
Line voltage	V_{AC}	110 / 230 V_{RMS}
Line frequency	f_{AC}	50 / 60 Hz
Maximum line current	$I_{AC,RMS\ max}$	16 A
Maximum load conditions	$P_{o,\ max}$	3 kW
Maximum output power of each cell	$P_{cell,\ max}$	1 kW
Converters switching frequency	f_{SW}	60 kHz
Average DC-link voltage	V_C	400 V_{DC}
Maximum DC-link voltage	$V_{C,\ max}$	450 V
Maximum peak-to-peak ripple of PFC stage inductor currents	$\Delta i_{Lj,\ pk\text{-}pk}$ (max)	2.8 A
Relative peak-to-peak ripple of BCR stage inductor currents	$\Delta i_{Li,\ pk\text{-}pk}$ (%)	< 90 %
Relative peak-to-peak ripple of line voltage (%)	$\Delta v_{AC,\ pk\text{-}pk}$(%)	< 2 %
Relative peak-to-peak ripple of the DC-link capacitor voltage (%)	$\Delta v_{C,\ pk\text{-}pk}$ (%)	< 5 %
Relative peak-to-peak ripple of the battery voltage (%)	$\Delta v_{Bat,\ pk\text{-}pk}$(%)	< 1 %
Battery voltage range	V_{Bat}	200 – 380 V
Maximum battery current	$I_{Bat,\ max}$	8 A

Table 2.1. Design specifications.

2.1.3 Interleaving technique

The application of the interleaving technique of different switching converters connected in parallel is highly recommended to reduce the ripple exhibited by their common input and output currents and voltages [43], this allowing a high reduction of filtering components' size. This technique consists in phase-shifting 360º/N the control signals with the same switching frequency of N parallel converters. This fact produces a ripple harmonic cancelation effect over the common input and output currents and voltages entailing a reduction of the residual ripple and an increment of its exhibited switching frequency up to N times the original switching frequency.

For example, the PFC stage that is composed by three parallel and interleaved bidirectional boost converters as depicted in Fig. 2.2 implies that $i_{INT1}(t)$ is defined as follows:

$$i_{INT1}(t) = \sum_{j=1}^{j=3} i_{Lj}(t) \tag{2.1}$$

where $i_{Lj}(t)$ stands for the current of inductor L_j where subscript j can be 1, 2 or 3.

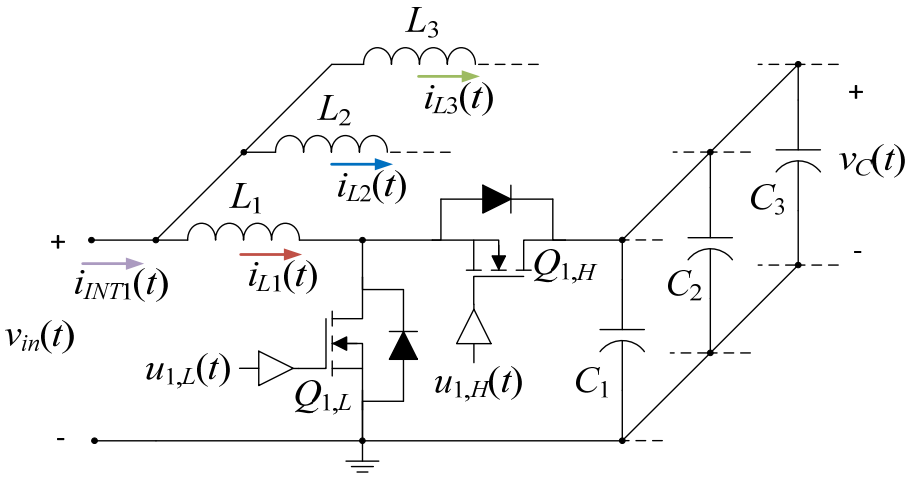


Fig. 2.2. Parallel connection of the PFC bidirectional boost converters.

If control signals $u_{j,L}(t)$ with a switching period T_{SW} are phase-shifted 360º/3=120º respectively, at time t_1 they can eventually present the form depicted in Fig. 2.3.a while the corresponding inductor currents $i_{Lj}(t)$ and total current $i_{INT1}(t)$ can be represented as in Fig. 2.3.b. It is clear that the ripple amplitude of $i_{INT1}(t)$ is lower than the exhibited by $i_{Lj}(t)$ due to the ripple harmonic cancelation effect commented previously. In addition, it can be observed how the residual switching frequency of $i_{INT1}(t)$ is three times the original f_{SW} (=1/T_{SW}) since the resulting switching period has become one third of the original switching period T_{SW}.

The ripple reduction can be quantified by means of the ripple harmonic cancellation function (F_{RHC}) [43] which defines the net ripple produced by N interleaved cells in terms of the amplitude of a single cell's ripple. In this case, N=3 and, in consequence, function F_{RHC} is given by the following expression:

$$F_{RHC}(D) = \begin{cases} 1 - \dfrac{2D}{1-D} & \text{if} \quad 0 \le D \le \dfrac{1}{3} \\ \dfrac{6D-2}{3D} - \dfrac{3(D+1)-4}{3(1-D)} & \text{if} \quad \dfrac{1}{3} < D < \dfrac{2}{3} \\ 1 + \dfrac{2(D-1)}{D} & \text{if} \quad \dfrac{2}{3} \le D \le 1 \end{cases} \tag{2.2}$$

where D corresponds to the ratio between voltage V_1 and voltage V_2 of the interleaved converters.

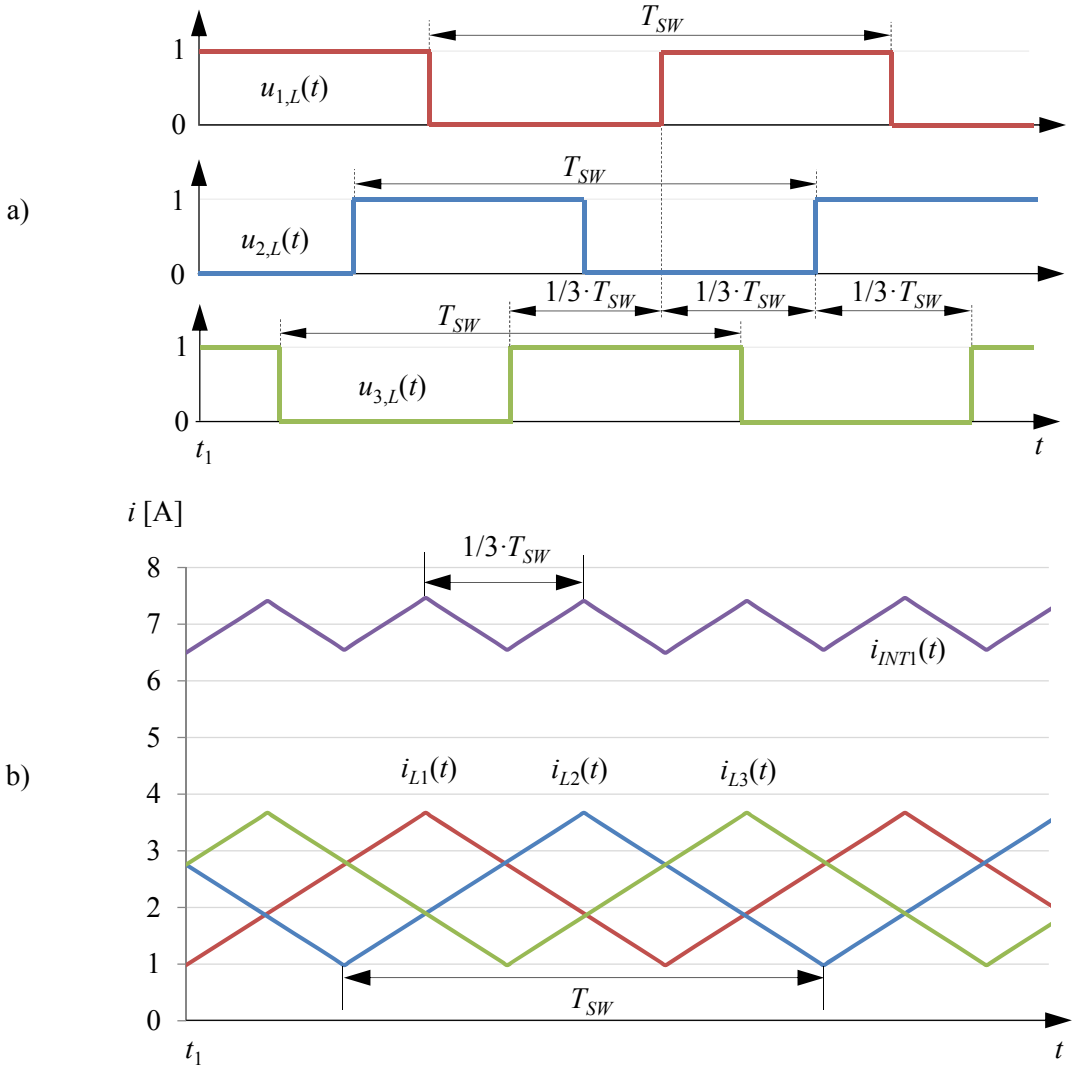


Fig. 2.3.Interleaved waveforms of the PFC stage. a) Phase-shifted control signals. b) Inductor currents $i_{Lj}(t)$ and total current $i_{INT1}(t)$

In the particular case of the PFC stage V_1=$v_{in}(t)$ and V_2=$v_C(t)$, while for the BCR stage V_1=$v_{Bat}(t)$ and V_2=$v_C(t)$ because the second stage can be analysed by mirroring the PFC stage.

$$D = \frac{V_1}{V_2} \tag{2.3}$$

The resulting plot of function $F_{RHC}(D)$ defined by (2.2) is depicted in Fig. 2.4. It can be observed how this function is null at D=1/3 and D=2/3, this implying that the net ripple is completely cancelled in these specific operating conditions.

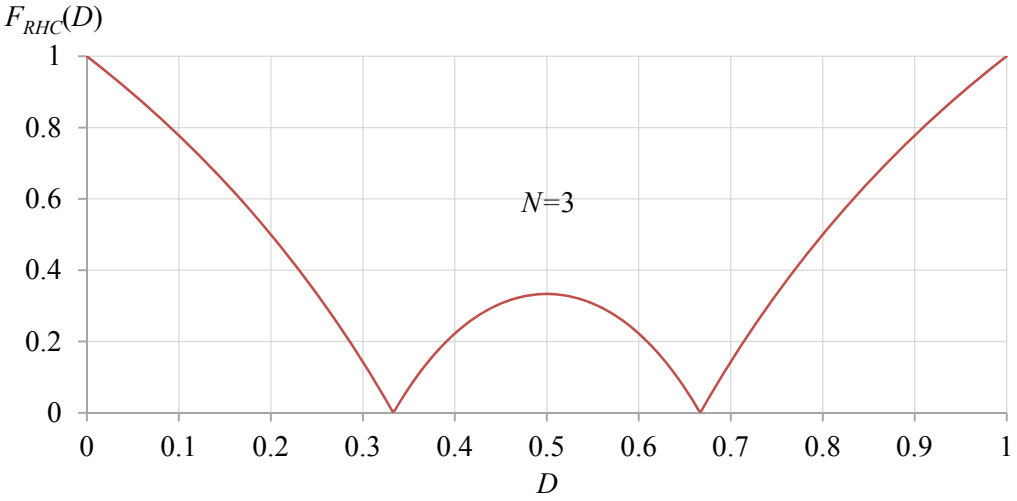
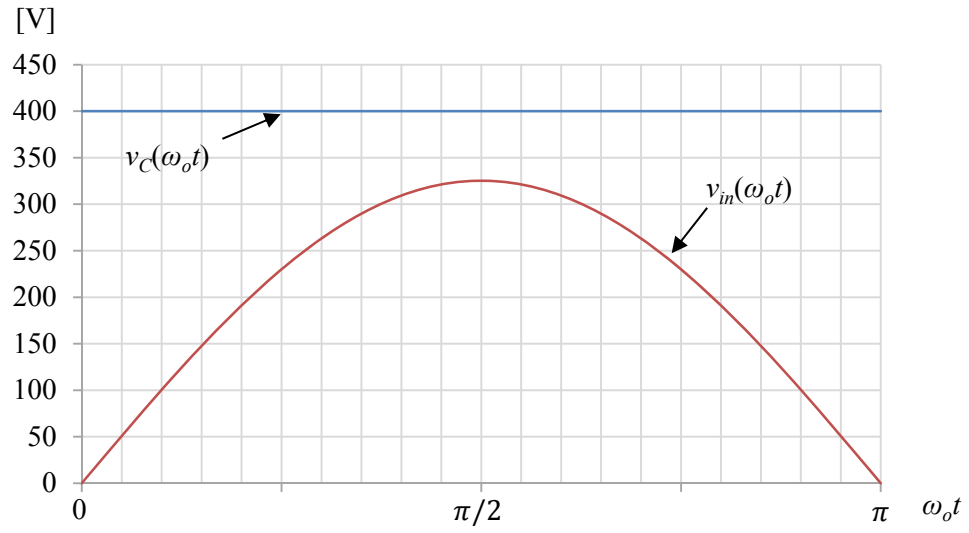


Fig. 2.4. Ripple harmonic cancellation function $F_{RHC}(D)$ for three interleaved cells.

a)



b)

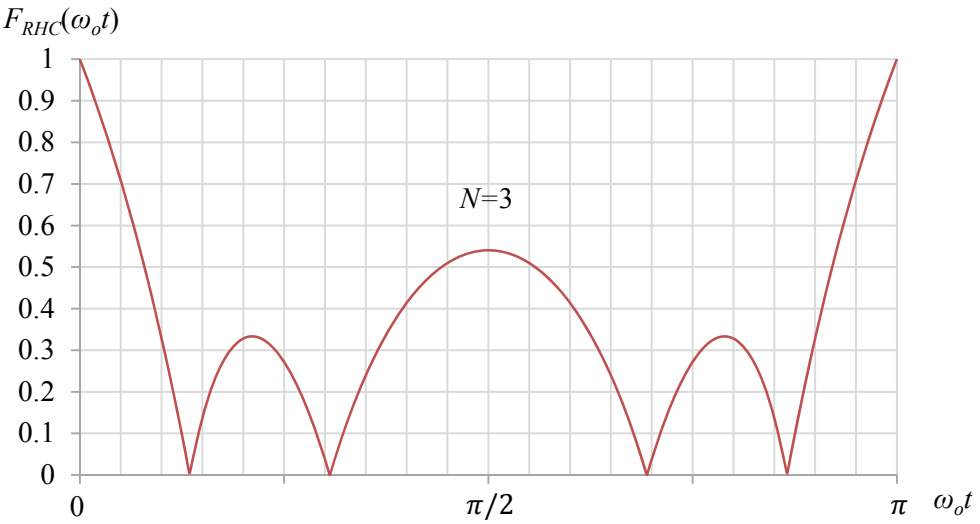


Fig. 2.5. PFC stage case for high line voltage conditions (230 V_{RMS}). a) Theoretical rectified input voltage and DC-link voltage over one half-line cycle. b) Resulting ripple harmonic cancellation function over one half-line cycle.

According to the voltage ranges defined in Table 2.1, it is possible to define the operation range of each stage. For the PFC stage, ratio D varies cyclically over one half-line cycle between 0 and 0.81 approximately since the rectified input voltage presents a minimum voltage of 0 V and a maximum of 325 V for high voltage line conditions (230 V_{RMS}) as depicted in Fig. 2.5.a. Assuming that the DC-link voltage v_C is flat with value V_C, $F_{RHC}(\omega_o t)$ results as illustrated in Fig. 2.5.b, where ω_o is $2\pi f_{AC}$.

The analysis is very similar for the BCR stage. Fig. 2.6 depicts the three parallel buck converters of the BCR stage, this implying that $i_{INT2}(t)$ is defined by the sum of all inductor current $i_{Li}(t)$, where subscript i can be 4, 5 or 6.

$$i_{INT2}(t) = \sum_{i=4}^{i=6} i_{Li}(t) \tag{2.4}$$

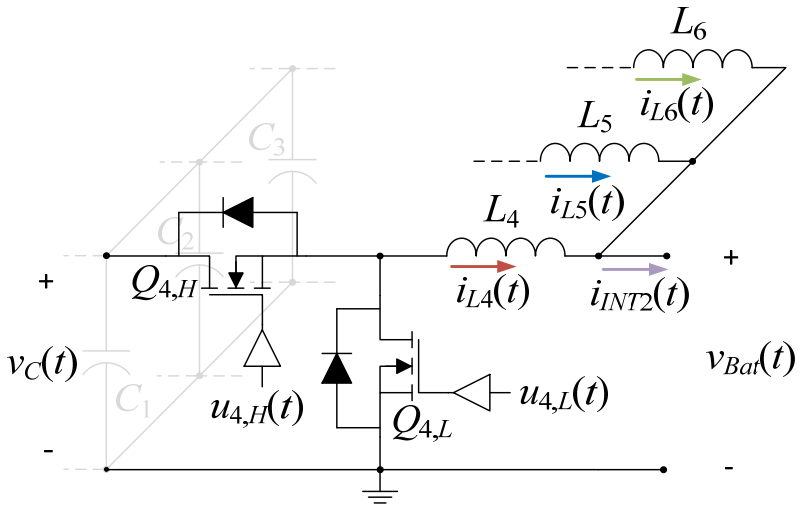


Fig. 2.6. Parallel connection of the bidirectional buck converters of the BCR stage.

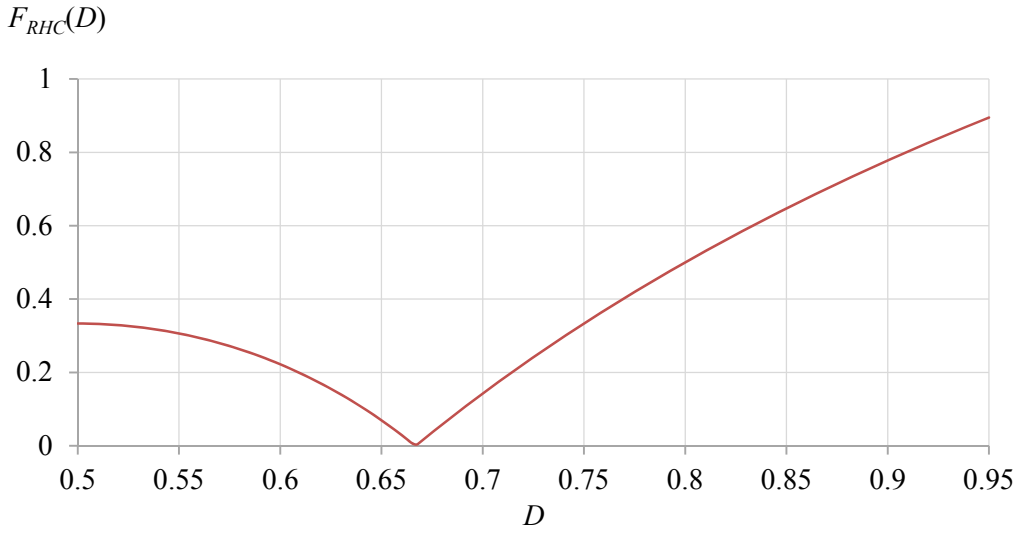


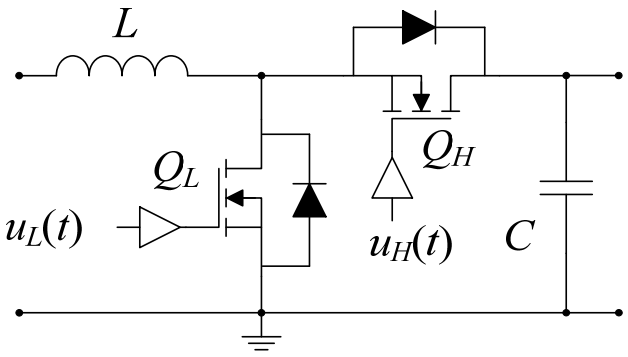
Fig. 2.7. Parallel connection of the bidirectional buck converters of the BCR stage.

Ratio D is expected to vary from 0.5 to 0.95 on the BCR stage because the DC-link voltage is expected to exhibit an almost constant value of V_C=400 V_{DC} while the minimum and maximum voltages of the battery are 200 V and 380 V respectively. Therefore, function $F_{RHC}(D)$ of the BCR stage results as depicted in Fig. 2.7.

2.1.4 Converters' bidirectional capability

To enable the bidirectional capability of the power flow, the most efficient solution, but more complex regarding its driving, is to switch two MOSFETs synchronously. As it can be observed in Fig. 2.8, one of the MOSFETs is placed in the low-side position (Q_L) and the other one is placed in high-side (Q_H). To allow the current flow through the MOSFETs' channels, their respective control signals have to be complementary, i.e. $u_L(t)=\overline{u_H}(t)$, and a dead-time should be introduced between them to avoid producing a short-circuit from the drain's high-side MOSFET node to the ground during switching transitions. However, in this work a different solution has been implemented to address the converters' bidirectional capability. A diode has been placed in series to each MOSFET and an extra diode has been connected in antiparallel with them as illustrated in see Fig. 2.8.

a)



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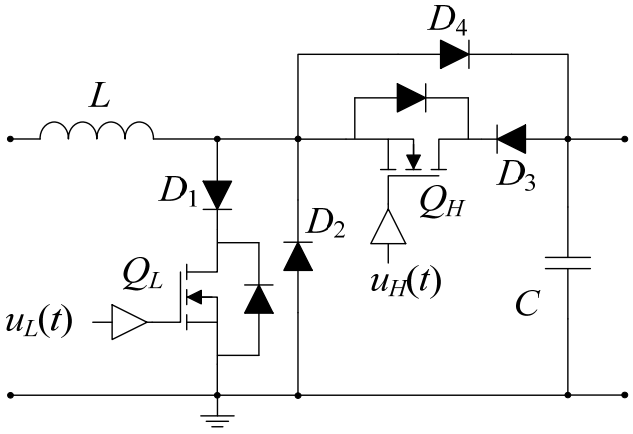


Fig. 2.8. Bidirectional boost converter. a) Using two synchronous MOSFETs. b) Adopted alternative.

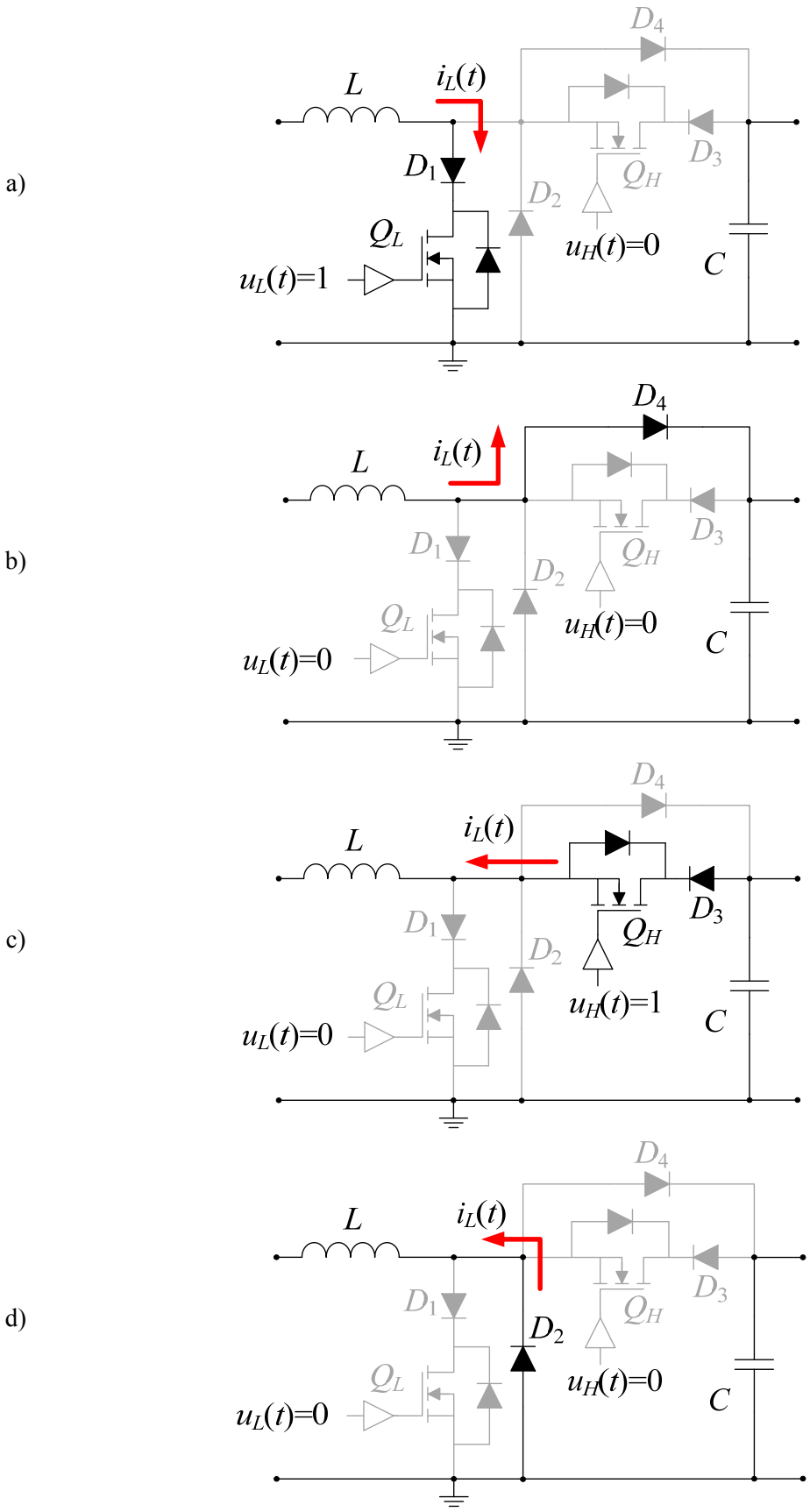


Fig. 2.9. Converters' asynchronous operation with the adopted alternative exemplified in a boost converter. Stepping up mode. a) On state. b) Off state. Stepping down mode. c) ON-state. d) OFF-state.

Although this solution is more expensive, bulkier and less efficient due to the presence of an extra diode in series to each MOSFET, it is simpler and the controlled switches can be driven independently. In fact, the converter can be controlled similarly to an asynchronous converter in both directions of the power flow due to the free-wheeling diodes D_2 and D_4 (see Fig. 2.9). Moreover, this solution allows the use of MOSFETs with slow recovery body diodes since their forward conduction is blocked by diodes D_1 and D_3.

2.1.5 Control stage structure

The control stage is divided into four different blocks as it can be seen in Fig. 2.10. The most important part of the control stage is the TMS320F28335 DSC from TEXAS INSTRUMETS. The DSC will be used to sense the conditioned sensing signals that come from the battery charger and compute the corresponding control action to be applied. The DSC will generate six control signals and four additional signals which are related to the direction of the power flow. All these signals are introduced to a logic circuitry that allows sending the previously mentioned control signals to the corresponding drivers as required.

Besides, the grid-synchronised rectifier will be also controlled from the DSC. An analogue circuit will be used to identify the sign of the AC voltage. Special attention will have to be taken at the vicinity of the zero-crossing instant of the line voltage to avoid short-circuiting the rectified input voltage to the ground or the AC voltage with itself. It is worth commenting also that for V2G operation, the PFC stage should stop charging its inductors before opening the controlled switches of the rectifier. Otherwise, any stored energy in these inductors could generate an important voltage peak on the rectified voltage node.

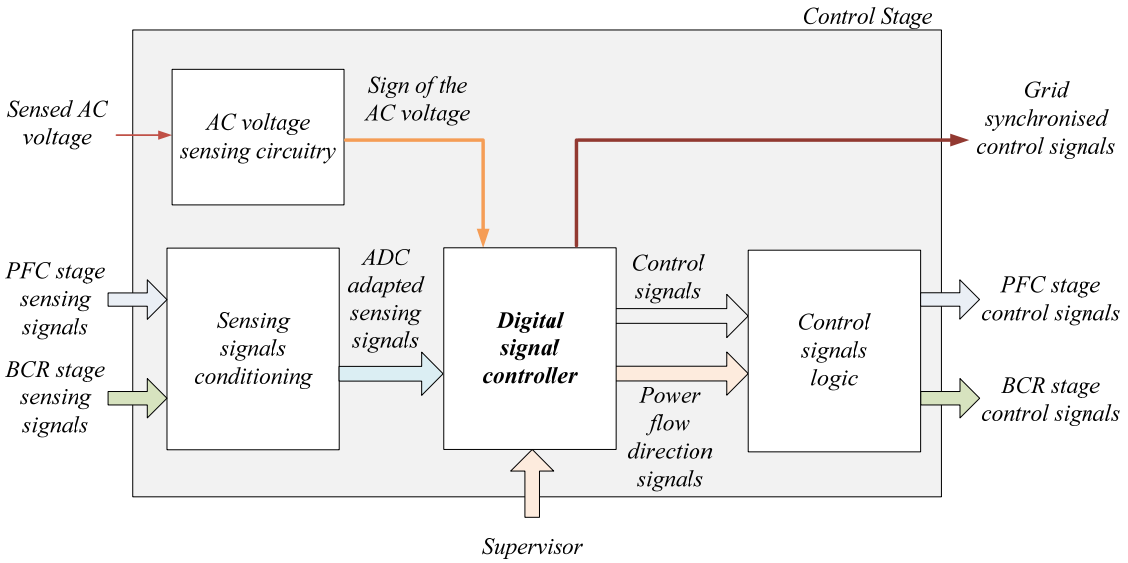


Fig. 2.10. General structure of the control stage.

2.2 Design of the power factor correction stage

The PFC stage is composed by three interleaved bidirectional boost cells like the one depicted in Fig. 2.11. Two voltage dividers have been employed to sense the rectified input voltage and DC-link voltage while one Hall-effect has been used to sense each inductor current.

To oversize the components, an efficiency of η_1=96% has been estimated for the PFC stage while a η_2=97% has been estimated for the second stage. The cascaded connection of both converters results in an estimated total efficiency of η=93%, being this latter the one with which the PFC stage has been designed and represented by the symbol η.

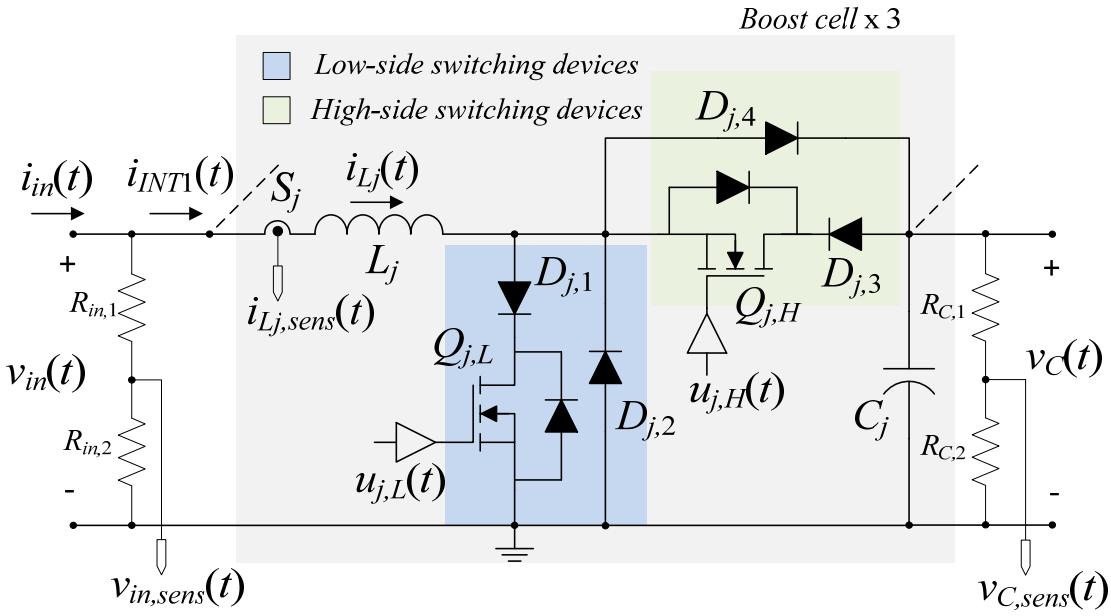


Fig. 2.11. Bidirectional boost/buck cell of the PFC stage.

2.2.1 PFC inductor design

The peak and *RMS* values of the inductor current can be calculated with the following expressions, which do not consider the peak-to-peak ripple of the inductor current.

$$I_{Lj,pk(\max)} = \frac{\sqrt{2}P_{cell,\max}}{\eta V_{AC}} \tag{2.5}$$

$$I_{Lj,RMS(\max)} = \frac{P_{cell,\max}}{\eta V_{AC}} \tag{2.6}$$

These expressions result in 6.61 A and 4.68 A for the peak and *RMS* current values respectively, this implying that the peak and *RMS* values of current $i_{in}(t)$ are 19.83 A and 14.04 A respectively.

The minimum required inductor can be calculated from the maximum allowed peak-to-peak current ripple $\Delta i_{Lj,\ pk\text{-}pk\ (\max)}$ with the following expression [45].

$$L_j = \frac{V_C}{4 f_{SW} \Delta i_{Lj,\,pk-pk\,(\max)}} \tag{2.7}$$

Thus, although the theoretical value results in L_j=595 μH, the final inductors exhibit an approximate inductance of 620 μH and have been realized by making 83 turns around three single 77439-A7 Kool Mμ cores from MAGNETICS with 12 wires of type AWG 29.

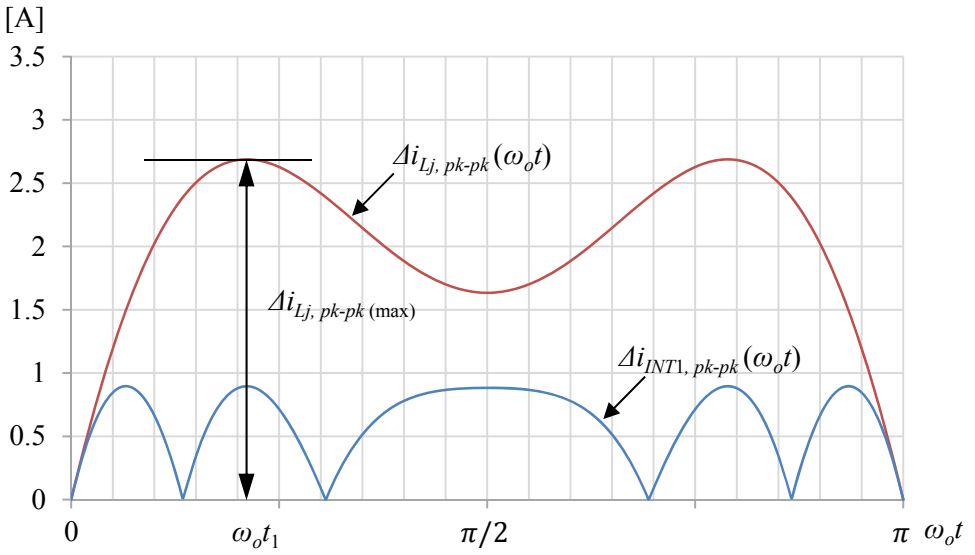
Expression (2.7) can be easily deduced from the definition of the inductor current ripple exhibited by a single boost converter which is annotated in (2.8). It can be demonstrated that the maximum ripple is given when the value of the rectified input voltage $v_{in}(t)$ is one half of the DC-link voltage $v_C(t)$ [43].

$$\Delta i_{Lj,\,pk-pk}(t) = \frac{v_{in}(t)}{L_j f_{sw}}\left(1 - \frac{v_{in}(t)}{v_C(t)}\right) \tag{2.8}$$

Hence, assuming that the maximum current is reached when the value of the rectified input voltage corresponds to $V_{AC}\sqrt{2}$ and the DC-link voltage adopts its average value V_C, it is possible to calculate the peak value of the inductor current (considering now its ripple). In this case conditions, expression (2.8) results in a peak-to-peak current ripple of 1.63 A. Therefore, the maximum peak current, which corresponds to the sum of $i_{Lj,pk(max)}$ and one half of the previously calculated current ripple, results in 7.43 A.

Moreover, Fig. 2.12 compares graphically both peak-to-peak current ripple amplitudes $\Delta i_{Lj,pk\text{-}pk}(\omega_o t)$ and $\Delta i_{INT1,pk\text{-}pk}(\omega_o t)$ over one half line cycle. For the sake of simplicity, it has been assumed that the DC-link voltage is constant. The first one is directly obtained from expression (2.8) where the inductance value L_j has been substituted by 620 μH, whereas the second one is the multiplication of $\Delta i_{Lj,pk\text{-}pk}(\omega_o t)$ with function $F_{RHC}(\omega_o t)$, which has been previously illustrated in Fig. 2.5.b, due to the interleaving technique. As it can be observed, the maximum peak-to-peak ripple amplitude of each individual inductor current $\Delta i_{Lj,pk\text{-}pk}(\omega_o t)$ reaches almost 2.7 A at $\omega_o t_1$. This value corresponds to a relative current ripple of 67.5 % with respect the local average current $I_{Lj}(\omega_o t)$ which is 4 A approximately under full load conditions (see Fig. 2.12.b). However, the maximum amplitude exhibited by $\Delta i_{INT1,pk\text{-}pk}(\omega_o t)$ is 0.88 A approximately while the local average current $I_{INT1}(\omega_o t)$ is around 12 A. In consequence, the relative peak-to-peak rectified input current ripple is lower than 7.5 %.

a)



b)

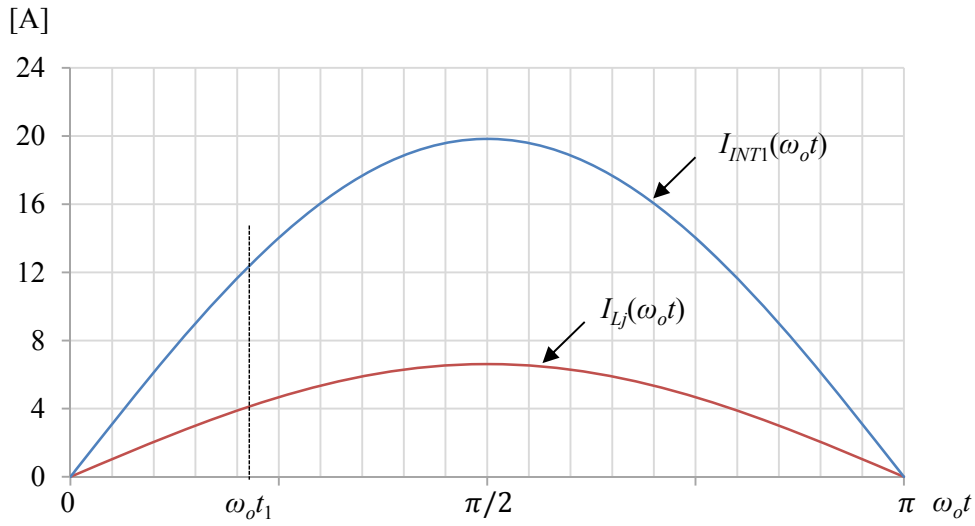


Fig. 2.12. Graphic comparison over half line cycle between a) peak-to-peak current ripple amplitudes $\Delta i_{Lj,pk\text{-}pk}(\omega_o t)$ and $\Delta i_{INT1,pk\text{-}pk}(\omega_o t)$, b) local average currents $I_{Lj}(\omega_o t)$ and $I_{INT1}(\omega_o t)$ under full load conditions.

2.2.2 DC-link capacitor design

Since the hold-up time is not strictly important in battery charging applications, the DC-link capacitor has been designed according to the specified relative voltage ripple by means of the following expression which is intensively used in the industry.

$$C = 3C_j = \frac{P_{o,\max}}{2\pi f_{AC} \Delta v_{C,pk-pk}(\%) V_C^{\,2}} \tag{2.9}$$

Although the previous equation leads to a theoretical capacitor of 1194 µF for f_{AC}=50 Hz, the finally implemented DC-link capacitor consists of:

- Twelve high voltage electrolytic capacitors of 100 µF whose manufacturer reference is EKXJ451ELL101MMP1S from NIPPON CHEMIN-CON.

- Six film capacitors of 1.5 μF whose manufacturer reference is B32654A6155J000 from EPCOS/TDK.
- Twenty-four ceramic capacitors of 220 nF whose manufacturer reference is CGA8M1X7T2J224K200KC from TDK.

The parallel connection of all the previous capacitors results in an approximate total DC-link capacitance of 1214 μF. This capacitance implies that the DC-link voltage exhibits a maximum relative voltage ripple of 4.92 %. Hence, the expected maximum ($V_{C,DC+pk}$) and minimum ($V_{C,DC-pk}$) voltage of the DC-link in steady-state and full load conditions can be calculated as follows.

$$V_{C,DC\pm pk} = V_C\left(1 \pm \frac{\Delta v_{C,pk-pk}(\%)}{2}\right) \tag{2.10}$$

Therefore, the resulting maximum and minimum voltage are 410 V and 390 V respectively. These values are taken into account in the design process of the BCR stage.

2.2.3 PFC power switches design

To calculate the current stress of the power switches, it is especially important to note that all the low-side switches and high-side switches are subjected to the same level of current respectively. This means that $Q_{j,L}$, $D_{j,1}$ and $D_{j,2}$ of Fig. 2.11 have to handle the same current stress and, in consequence, $Q_{j,H}$, $D_{j,3}$ and $D_{j,4}$ too. However, the current will only circulate through some of them depending on the direction of the power flow.

2.2.3.1 Low-side switching devices

According to [105] the average and *RMS* current of the low-side switching devices can be calculated by the following expressions

$$i_{Low side,avg(\max)} = \frac{2\sqrt{2}P_{cell,\max}}{\pi\eta V_{AC}}\left(1 - \frac{\pi\sqrt{2}V_{AC}}{8V_C}\right) \tag{2.11}$$

$$i_{Low side,RMS(\max)} = \frac{P_{cell,\max}}{\eta V_{AC}}\sqrt{1 - \frac{8\sqrt{2}V_{AC}}{3\pi V_C}} \tag{2.12}$$

These expressions result in approximately 2.89 A and 2.60 A respectively for the peak and *RMS* current values. Moreover, the peak current supported by the power switches is 7.43 A, which has been calculated previously in the inductor design section. The manufacturer reference of the selected MOSFETs is IPW60R160C6 from INFINEON.

Besides, power diodes play an important role because the main disadvantage of hard switching and asynchronous continuous conduction mode (CCM) operation are the losses generated by the reverse recovery charge (Q_{rr}) of the switching diodes. For this reason, Silicon Carbide (SiC)

diodes have been preferred because they exhibit a lower Q_{rr} with respect their Silicon (Si) counterparts. In particular, both selected diodes are SiC diodes of type IDH10SG60C from INFINEON.

2.2.3.2 High-side switching devices

According to [105] the average and *RMS* current of the high-side switching devices can be calculated by the following expressions

$$i_{High\ side,avg(\max)} = \frac{P_{cell,\max}}{\eta V_C} \tag{2.13}$$

$$i_{High\ side,RMS(\max)} = \sqrt{\frac{8\sqrt{2}\left(\frac{P_{cell,\max}}{\eta}\right)^2}{3\pi V_{AC} V_C}} \tag{2.14}$$

These expressions result in 2.69 A and 3.88 A respectively. However, the peak current is the same for both groups of switching devices, so that, the same MOSFET and SiC diodes have been selected for the high-side switching devices group.

2.2.4 PFC sensing circuitry

This section only gives the details about the sensing circuitry that is present in the power stage of the PFC. More details about how the sensing signals are introduced to the digital controller for their sampling are given afterwards.

2.2.4.1 Rectified input voltage divider

A voltage divider has been employed to measure the rectified input voltage. It has been designed according to the full scale voltage of the internal analogue-to-digital converter (ADC) of the DSC which is 3 V. The minimum required attenuation of the sensed input voltage signal is calculated according to the expected maximum input voltage.

$$g_{div1,\min} = \frac{V_{ADC,\max}}{\sqrt{2}V_{AC}} \tag{2.15}$$

$V_{ADC,\ max}$ stands for the full scale of the ADC. Thus, the minimum required attenuation $g_{div1,\min}$ results in $9.223 \cdot 10^{-3}$. To give a sufficient safety margin, the selected values for $R_{in,1}$ and $R_{in,2}$ are 680 kΩ and 5.6 kΩ respectively, leading to an attenuation of $8.168 \cdot 10^{-3}$. This value can easily be calculated by the following expression.

$$g_{div1} = \frac{R_{in,2}}{R_{in,1} + R_{in,2}} \tag{2.16}$$

2.2.4.2 Dc-link voltage divider

As well as for the input voltage measurement, a voltage divider has been employed to measure the DC-link voltage. In this case, the DC-link voltage is not expected to be higher than 450 V since the electrolytic capacitors of the DC-link cannot handle a higher voltage. This leads to the following minim required attenuation of the voltage divider.

$$g_{div2,\min} = \frac{V_{ADC,\max}}{V_{C,\max}} \tag{2.17}$$

The minimum required attenuation $g_{div2,\min}$ results in $6.667 \cdot 10^{-3}$. To give a sufficient safety margin, the selected values for $R_{C,1}$ and $R_{C,2}$ are 1 MΩ and 5.6 kΩ respectively leading to an attenuation of $5.569 \cdot 10^{-3}$.

2.2.4.3 Inductor current sensor

A Hall-effect current sensor LA 25-NP from LEM has been connected in series to each inductor of the PFC cells in order to sense each inductor current independently. This sensor has been configured with three turns in the primary winding since the maximum expected current to circulate through the inductors should be lower than 8 A. This configuration induces 3 mA in the secondary winding per 1 A flowing through the primary winding.

2.3 Design of the battery current regulation stage

The BCR stage is made up of three bidirectional buck cells connected in parallel like the one depicted in Fig. 2.13. In order to simplify further schematic circuits, each cell will be depicted with only two MOSFETs.

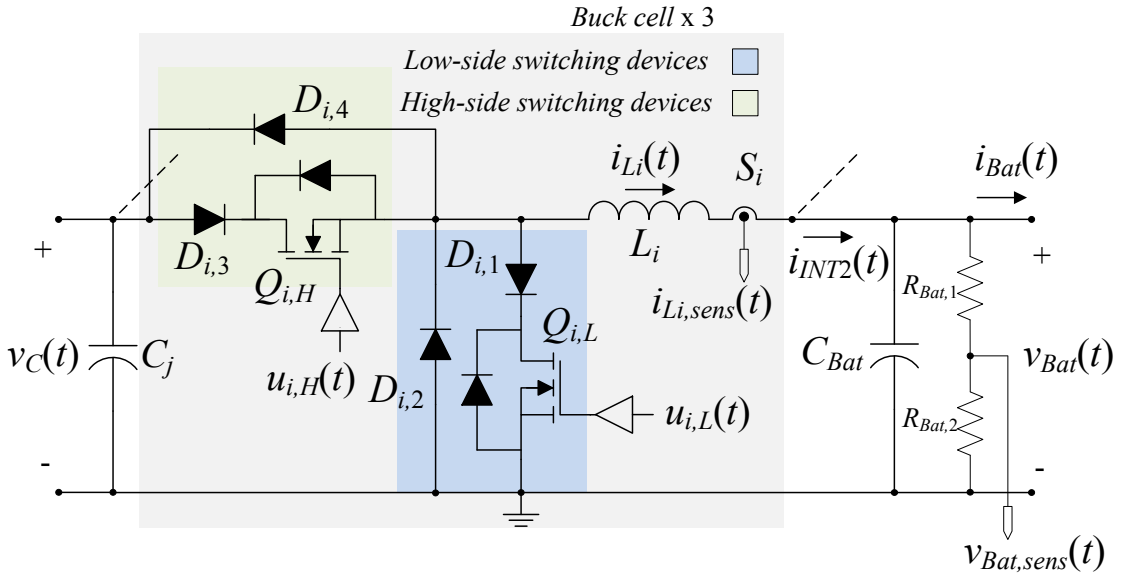


Fig. 2.13. Bidirectional buck cell of the BCR stage.

This stage is meant to operate in two different modes: CC and CV modes similarly to the battery charging profile depicted in Fig. 2.14.a. While the battery voltage is below the nominal voltage of the battery (380 V in this case), the charger has to deliver a constant current to the battery. Once the battery has reached its nominal voltage, the charger has to start operating in CV mode and reduce the current delivered to the battery accordingly until the battery is completely charged [66, 67]. This behaviour leads to a power profile similar to the one illustrated in Fig. 2.14.b.

An efficiency of 97% has been considered for the design of the second stage, which comes represented by symbol η_2.

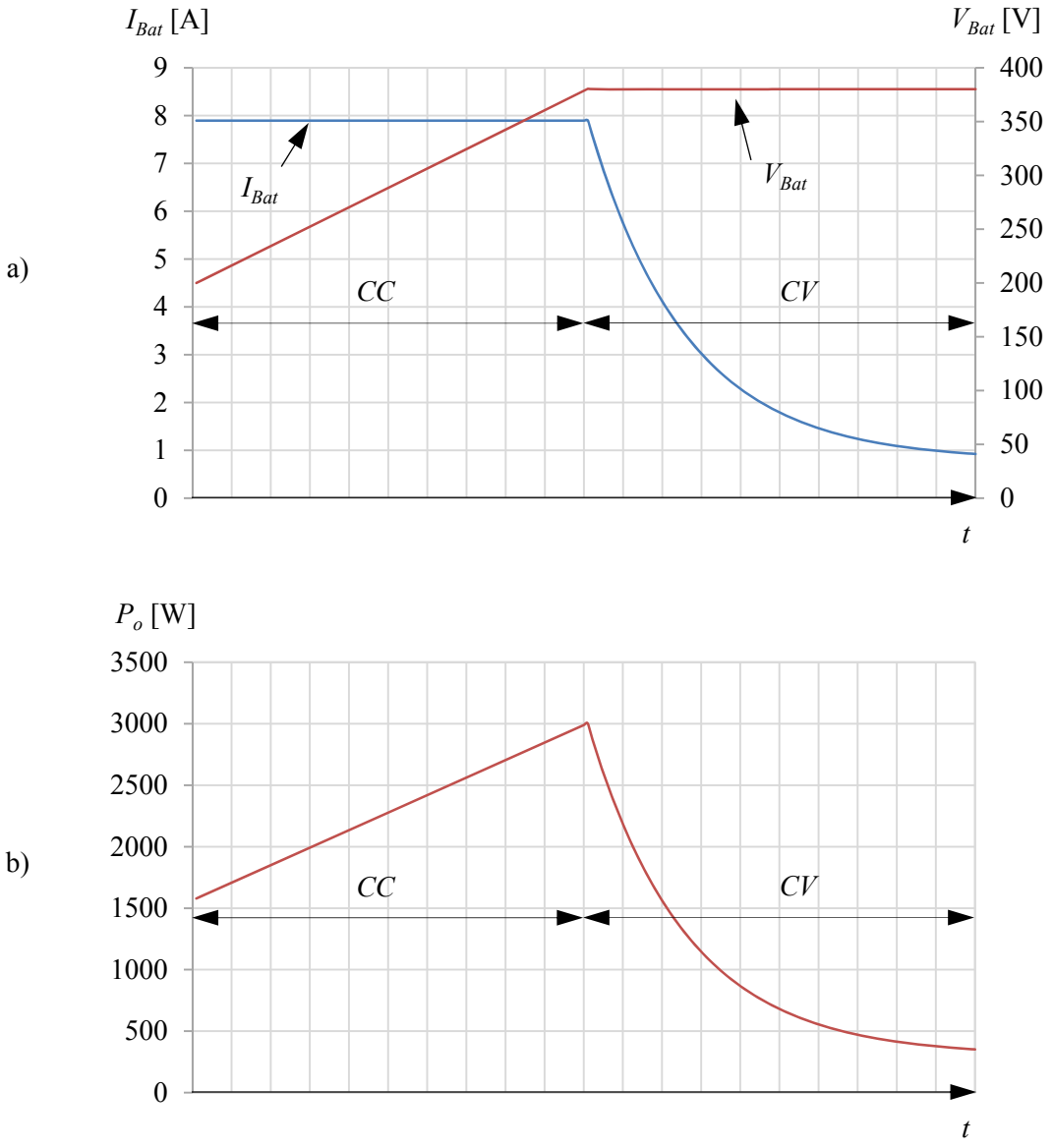


Fig. 2.14. Battery charging profile vs time. a) Battery current and voltage. b) Power delivered to the battery.

2.3.1 BCR inductor design

The maximum average value of the inductor current remains constant while the battery charger is operating in CC mode and it can be calculated by using the following expression.

$$i_{Li,avg(\max)} = \frac{P_{cell,\max}}{\eta_2 V_{Bat,\max}} \tag{2.18}$$

The previous expression results in 2.71 A of maximum average current.

Similarly to the previous case, the inductor is designed according to the maximum specified relative current ripple $\Delta i_{Li,pk\text{-}pk}(\%)$. Note from expression (2.19) that maximum amplitude of the inductor current ripple is also reached when the battery voltage is one half of the DC-link voltage.

$$\Delta i_{Li,\,pk-pk}(t) = \frac{\left(v_C(t) - v_{Bat}(t)\right) v_{Bat}(t)}{L_i f_{sw} v_C(t)} \tag{2.19}$$

Hence, the required inductor can be calculated as follows.

$$L_i = \frac{V_C}{4\Delta i_{Li,\,pk-pk}(\%)\, i_{Lj,avg(\max)} f_{SW}} \tag{2.20}$$

Although the theoretical inductance value results in L_i=683 µH, the final inductors present an approximate inductance of 720 µH and have been realized by making 85 turns around a 77439-A7 Kool Mµ core from MAGNETICS using 5 wires of type AWG 22.

Once the inductor has been defined, it is possible to calculate the peak value of its current taking into account its ripple in addition to the maximum DC-link voltage and the minimum battery voltage. It can be demonstrated that it results in a peak-to-peak current ripple value of 2.32 A. In consequence, the maximum expected peak current value is 3.87 A.

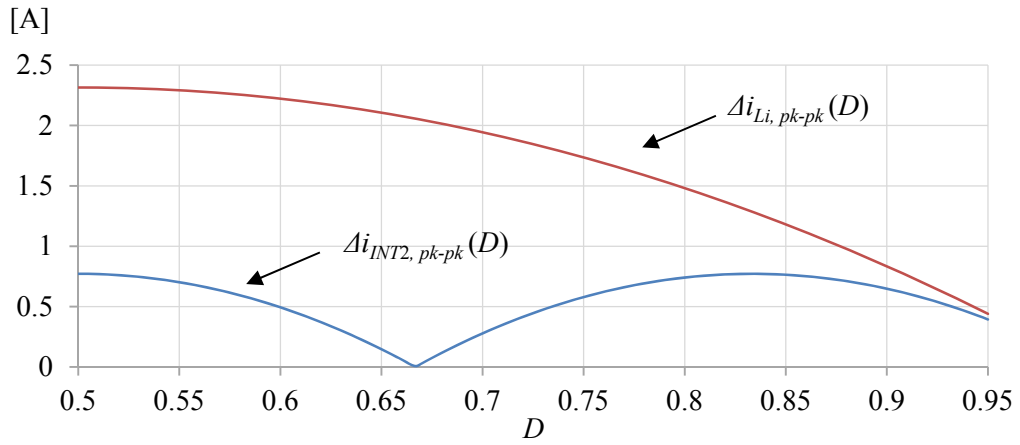


Fig. 2.15. Graphic comparison of peak-to-peak current ripple amplitudes $\Delta i_{Li,pk\text{-}pk}(D)$ and $\Delta i_{INT2,pk\text{-}pk}(D)$ for the operative range of the BCR stage.

Fig. 2.15 illustrates the expected peak-to-peak current ripple amplitudes $\Delta i_{Li,pk\text{-}pk}(D)$ and $\Delta i_{INT2,pkpk}(D)$ as a function of ratio D over the operative range of the BCR stage considering that the DC-link voltage is flat and L_i=720 µH. It can be demonstrated that the maximum relative peak-to-peak current ripple of a single inductor is around an 86 % with respect its average current value. However, the maximum ripple amplitude exhibited by $i_{INT2}(t)$ is only 0.77 A due to the interleaved operation, which corresponds to a 9.5 % with respect its average value.

2.3.2 Output capacitor design

A capacitor has been placed at the output of the system in order to filter the high frequency voltage ripple produced by the interleaved switching operation of the BCR stage cells. Its value can be calculated as follows

$$C_{Bat} = \frac{\Delta i_{INT2,\,pk-pk(\max)}}{2\pi\left(3f_{SW}\right)\Delta v_{Bat,\,pk-pk}\left(\%\right)V_{Bat,\min}} \tag{2.21}$$

where $\Delta i_{INT2,pk\text{-}pk(\max)}$ is 0.77 A as it has been seen in the previous section. Although the theoretically required minimum output capacitor results in 340 nF, one film capacitor of 330 nF with reference R463N333050M1K from KEMET and one electrolytic capacitor of 10 µF with reference 500BXC10MEFC12.5X20 from RUBYCON have been placed in parallel at the output terminals of each BCR stage cell.

2.3.3 BCR power switches design

Similarly to the previous case, all the components that correspond to the same group have to handle the same current stress. In this case, the peak current corresponds to 3.87 A as it has been seen in the inductor design section. The same MOSFETs and diodes as the PFC stage have been selected in this case.

2.3.3.1 Low-side switching devices

The maximum average current that has to be handled by the low-side switching devices is defined by the following expression, which results in 1.36 A.

$$i_{Low\,side,\,avg(\max)} = i_{Li,\,avg(\max)}\left(1-\frac{V_{Bat,\min}}{V_C}\right) \tag{2.22}$$

2.3.3.2 High-side switching devices

The maximum average current that has to be handled by the high-side switching devices is defined by the following expression, which results in 2.58 A.

$$i_{High\ side,\,avg(\max)} = i_{Li,\,avg(\max)}\frac{V_{Bat,\max}}{V_C} \tag{2.23}$$

2.3.4 BCR sensing circuitry

This section gives details about the sensing circuitry present in the battery current regulation stage. More details about how the sensing signals are introduced to the digital controller for their sampling are given afterwards.

2.3.4.1 Battery voltage divider

Similarly to the rectified input and DC-link voltages, the battery voltage is measured with a voltage divider. The maximum expected battery voltage is 380 V, so that the minimum required attenuation $g_{div3,\min}$ is defined as follows.

$$g_{div3,\min} = \frac{V_{ADC,\max}}{V_{Bat,\max}} \tag{2.24}$$

The previous expression results in $7.895 \cdot 10^{-3}$. To give a sufficient safety margin, values for $R_{Bat,1}$ and $R_{Bat,2}$ have been selected as 820 kΩ and 5.6 kΩ respectively, so that the resulting attenuation is $6.783 \cdot 10^{-3}$.

2.3.4.2 Inductor current sensor

As well as in the PFC stage, a Hall-effect current sensor LA 25-NP from LEM has been employed in each cell in order to sense each inductor current independently. Three turns in the primary winding have been also selected.

2.4 Design of the grid-synchronised rectifier

2.4.1 Power switches

The full-bridge synchronous rectifier has been designed to handle the sum of currents of all the PFC cells, which reaches an approximate peak value of 20 A and an *RMS* value of 14 A. Four MOSFETs with reference IPW60R041C6 from INFINEON have been selected due to their very low on-state resistance to perform the rectification as depicted in Fig. 2.16. Note that only two MOSFETs are switched-on during each half-line cycle and their activation only depends on the sign of the AC voltage. All MOSFETs are temporally switched off during the zero crossing transition of the AC voltage to avoid an eventual short-circuit. Besides, one diode STTH6004W from ST has been placed in parallel with each MOSFET to reinforce the rectification operation during the battery charging process.

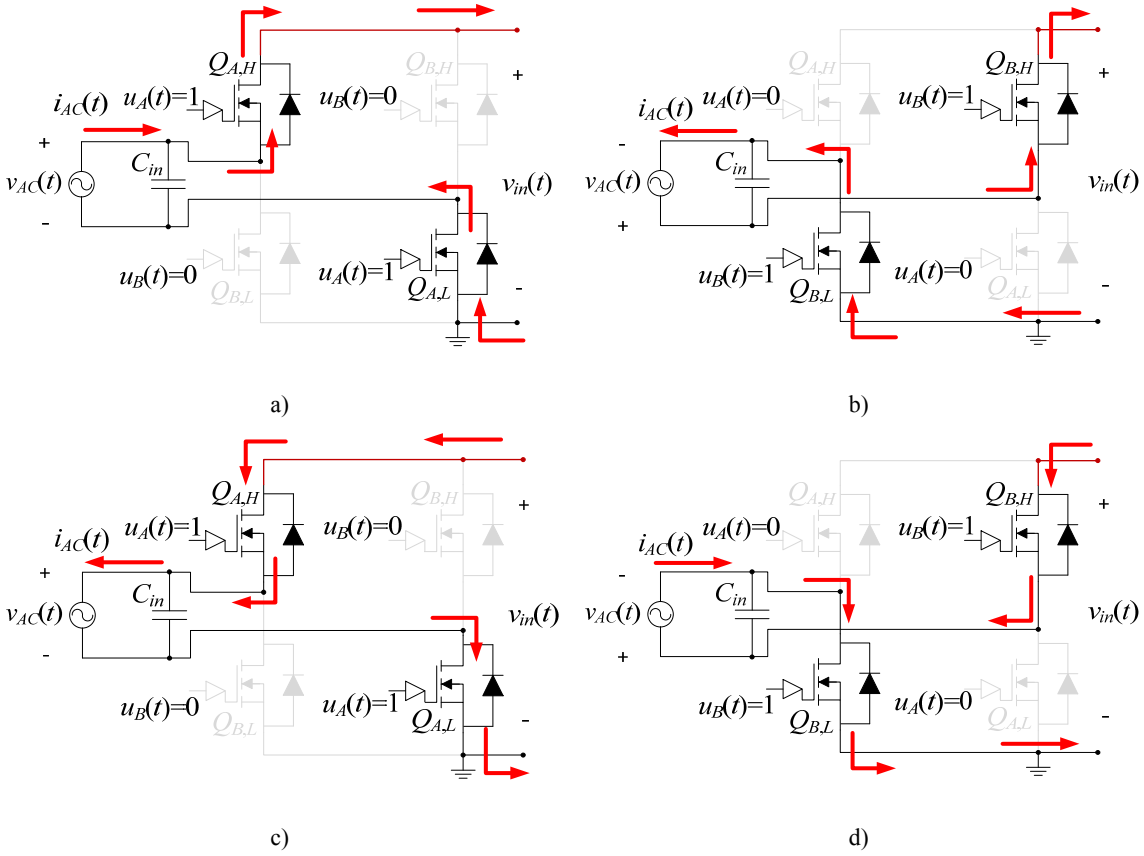


Fig. 2.16. Bidirectional operation of the full-bridge grid-synchronised rectifier: $u_A(t)$=1 and $u_B(t)$=0 when $v_{AC}(t)$>0, $u_A(t)$=0 and $u_B(t)$=1 when $v_{AC}(t)$<0. G2V operation a) $v_{AC}(t)$>0, b) $v_{AC}(t)$<0. V2G operation a) $v_{AC}(t)$>0, b) $v_{AC}(t)$<0.

2.4.2 Input capacitor design

Although most of applications include an EMI filter between the line connection and the electronic equipment, this filter was omitted in this work and was considered out of the scope of the thesis. However, a capacitor with a relatively low capacitance has been placed at the input of the system in order to filter the high frequency ripple of the AC input voltage generated by the interleaved switching operation of the PFC stage cells. It is important to remark that this capacitor should be designed together with the EMI filter since they would be connected directly in parallel.

This capacitor should remove the high frequency voltage ripple produced by the current ripple of $i_{INT1}(t)$ which is expected to present a maximum amplitude $\Delta i_{INT1,pk\text{-}pk(\max)}$=0.88 A. In addition, it is important to remark that the frequency of this current ripple is three times the switching frequency of each cell.

$$C_{in} = \frac{\Delta i_{INT1,\,pk-pk(\max)}}{2\pi\left(3f_{SW}\right)\Delta v_{AC,\,pk-pk}\left(\%\right)V_{AC}} \tag{2.25}$$

Although the previous expression results in 169.15 nF for C_{in}, the selected capacitance value is 680 nF due to its good performance and because it is sufficiently low to not distort the input

current. The manufacturer reference of the employed capacitor is 2222 338 40684 from VISHAY BC COMPONENTS.

2.5 Design of the control stage

In this section, a more detailed description of the control stage hardware configuration is provided. In particular, Fig. 2.17 depicts the complete signal connection between the battery charger and the control stage as well as between the blocks of the control stage. As it will be seen, this section only gives information about the connection of the DSC with the rest of the elements from the control stage. Details about the digital control algorithm are given in Chapter 4.

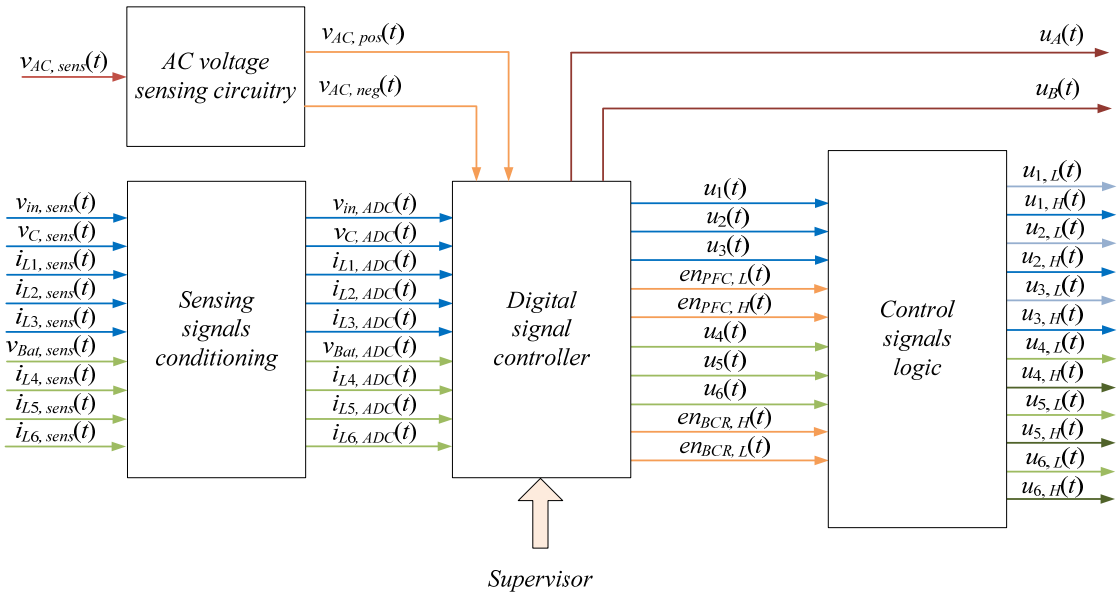


Fig. 2.17. Complete signal connection diagram of the control stage.

2.5.1 Sensing signals conditioning

All sensing signals that come from the power stage of the battery charger are conditioned accordingly to be connected to the analogue inputs of the TMS320F28335 DSC. A simplified schematic of the implemented circuit is depicted in Fig. 2.18.

On one hand, the three sensing voltage signals are connected to rail-to-rail operational amplifiers (OAs) which are configured as voltage followers. A 100 Ω resistor is connected between the output of the OAs and the input of the ADCs of the DSC in order to compensate the low-impedance output of the OAs.

On the other hand, sensed inductor currents $i_{Lk,sens}(t)$, where index k is j for the PFC stage and i for the BCR stage, need to be adapted to the operating range of the internal ADCs of the DSC that is from 0 V to 3 V. The employed Hall-effect current sensors generate a positive current on

the secondary winding when the current that is flowing through the primary winding is also positive. In contrast, a negative current in induced on the secondary winding when the primary current is negative. A resistor R_{Sk} is employed to transform this current in the secondary winding into a voltage, which is amplified afterwards to be sent to the DSC. However, the resulting signals cannot be sent directly to the DSC because this signal would be negative for negative currents on the primary winding of the current sensor. A simple circuit based on OAs has been implemented to solve this issue, so that signals that are sampled by the ADC corresponding to inductor currents are defined as follows:

$$i_{Lk,ADC}(t) = i_{Lk,sens}(t) R_{Sk} \left(\frac{5}{11} \right) + 1.5\,\text{V} \tag{2.26}$$

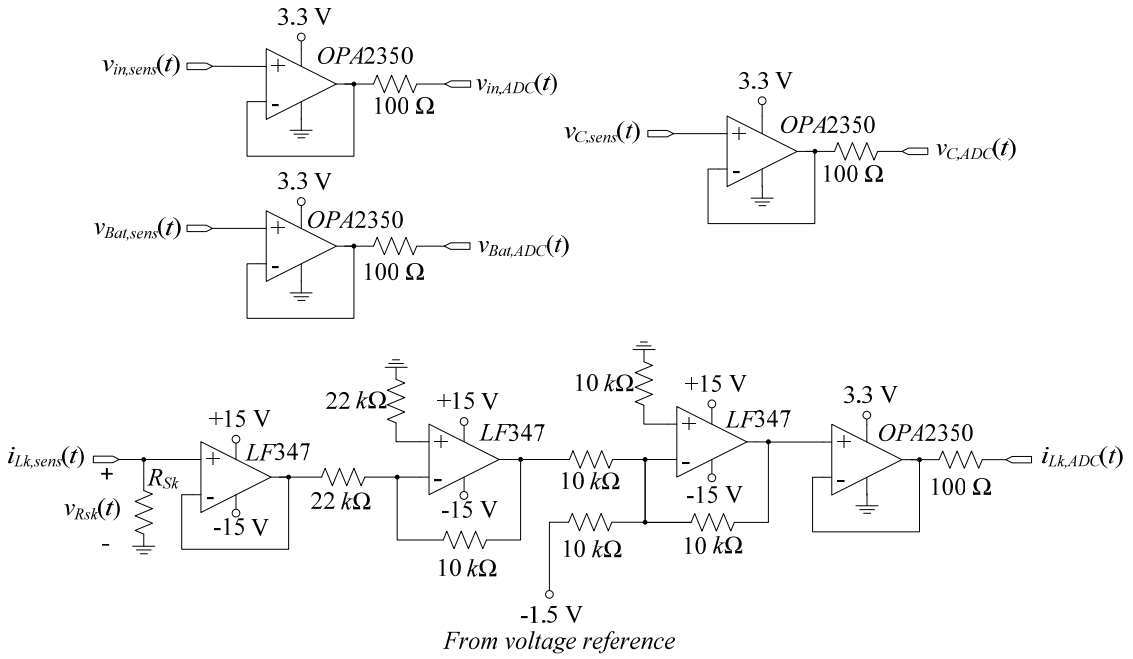


Fig. 2.18. Simplified scheme of the sensing signals conditioning block.

As it can be observed, an offset and a proportional gain have been introduced to allow sensing the inductor current in both directions. If $i_{Lk,sens}(t)$=0 A, signal $i_{Lk,ADC}(t)$ becomes 1.5 V, which is half of the full scale voltage of the ADCs. Despite the fact that this circuit has been implemented for both stages, resistors R_{Sk} are different in each one. While the value of resistors R_{Sj} for the PFC stage (k=j) is 120 Ω, resistors R_{Si} for the BCR stage are 220 Ω. Hence, it can be demonstrated that for the PFC stage, $i_{Lj,ADC}(t)$=0 V means that $i_{Lj}(t)$=-9.167 A while $i_{Lj,ADC}(t)$=3 V indicates that $i_{Lj}(t)$=9.167 A. Differently, $i_{Li,ADC}(t)$=0 V means that $i_{Li}(t)$=-5 A while $i_{Li,ADC}(t)$=3 V implies that $i_{Li}(t)$=5 A for the BCR stage cells.

2.5.2 Digital Signal Controller

The selected DSC for this thesis is a TMS320F28335 DSC from TEXAS INSTRUMENTS. It samples the information from the sensing signals conditioning stage and generates the corresponding PWM control signals $u_k(t)$ according to the programmed control laws. This DSC is a powerful platform for real-time control of power electronics systems due to its flash-memory and 32-bit floating point unit (FPU) architecture which allows a high speed execution of complex control algorithms.

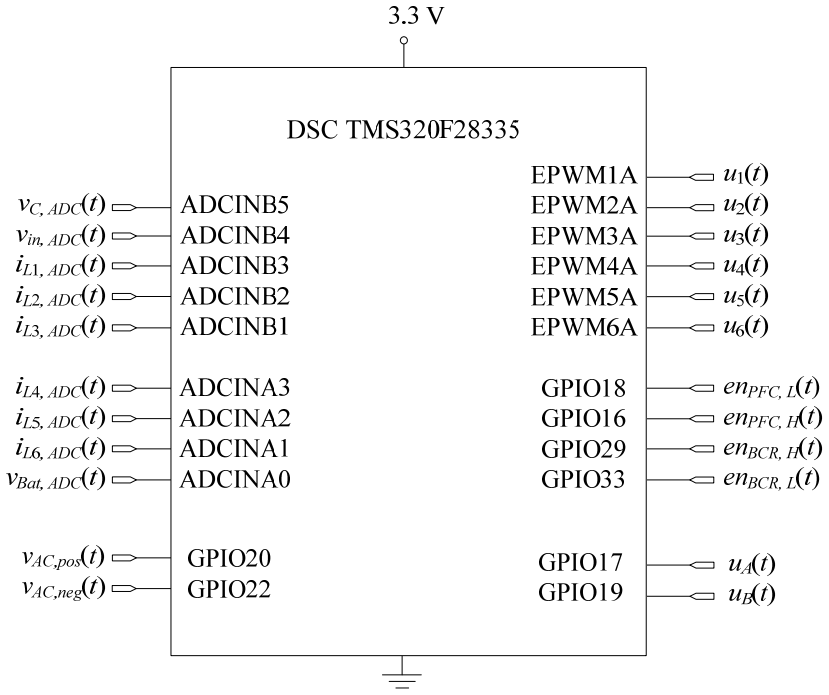


Fig. 2.19. Pin out connection of the DSC.

As it can be seen in Fig. 2.19, the six enhanced pulse width modulation (EPWM) modules of the DSC are employed to generate six control signals $u_k(t)$. Note that, despite the fact that there are twelve controlled switches in total in both cascaded-stages of the battery charger, only six control signals are sent to the logic control board. These six control signals are sent together with four extra digitals signals to the logic control block with the following purposes:

- $en_{PFC,L}(t)$ signal enables the G2V operation mode of the PFC stage cells. It allows control signals $u_j(t)$ to be sent to low-side controlled switches $Q_{j,L}$ of the PFC stage by means of signals $u_{j,L}(t)$.
- $en_{PFC,H}(t)$ signal enables the V2G operation mode of the PFC stage cells. It allows control signals $u_j(t)$ to be sent to high-side controlled switches $Q_{j,H}$ of the PFC stage by means of signals $u_{j,H}(t)$.

- $en_{BCR,H}(t)$ signal enables the G2V operation mode of the BCR stage cells. It allows control signals $u_i(t)$ to be sent to high-side controlled switches $Q_{i,H}$ of the BCR stage by means signals $u_{i,H}(t)$
- $en_{BCR,L}(t)$ signal enables the V2G operation mode of the BCR stage cells. It allows control signals $u_i(t)$ to be sent to low-side controlled switches $Q_{i,L}$ of the BCR stage by means signals $u_{i,L}(t)$.

These four enabling signals are employed to have more flexibility when enabling or disabling the MOSFETS' operation. The direction of the power flow would be defined by an external supervisor. However, it was omitted in this case and the direction of the power flows was instead pre-defined at the beginning of the control execution.

Besides, the grid-synchronised rectifier will be controlled by means of the identification of the AC voltage sign. One analogue circuit based on an AD629 has been designed to identify the AC voltage sign and send two digital signals to the DSC for a proper identification of the zero-voltage transition. Control signals $u_A(t)$ and $u_B(t)$ manage the grid-synchronised rectifier and they are sent through two general purpose input output (GPIO) pins. As it has been seen previously in Fig. 2.16, signals will be $u_A(t)$=1 and $u_B(t)$=0 for the positive half-line cycle, and $u_A(t)$=0 and $u_B(t)$=1 for the negative half-line cycle. They will never be activated at the same time and they will be both 0 around the zero-crossing instant.

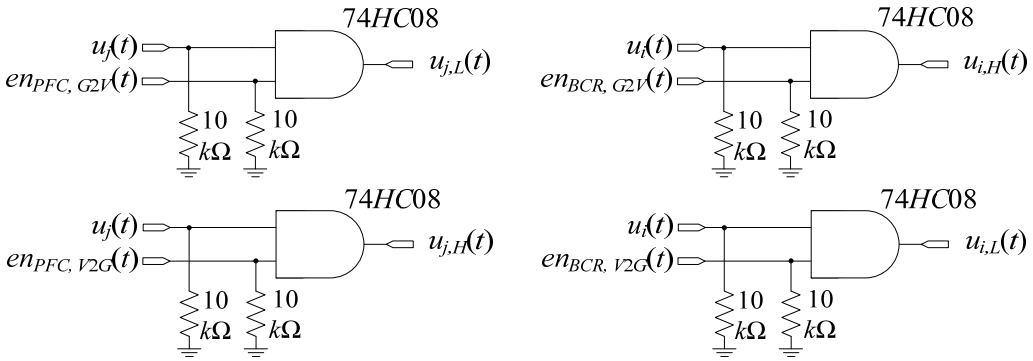


Fig. 2.20. Simplified scheme of the control signals logic block.

2.5.3 Control signals logic circuit

This block has been partially commented in the previous section. It receives control signals $u_k(t)$ and sends them to the correct MOSFET depending on the enabling signals which have been already explained. The enabling procedure is carried out by means of AND gates, whose inputs are pulled-down to ground by 10 kΩ resistors (see Fig. 2.20).

2.6 Summary

This chapter has focused on the design of the battery charger circuit according to different specifications which are common in the field of automotive industry. The proposed battery charger for EVs is suitable for slow charging applications because it has been designed for a rated power of 3 kW. The proposed system is composed by two-cascaded stages, which are configured by three interleaved converters. In particular, the first stage is configured by three boost converters and they are meant to pre-regulate the DC-link voltage and achieve a unity PF. The second stage is meant to match the voltage difference between the DC-link and the battery and to deliver the required current to the battery according to its voltage.

The chapter also includes an analysis regarding the cells' interleaving operation to predict the form of the resulting interleaved currents. Sensing signal requirements and their conditioning are also reported. Finally, a detailed description about the connection between the power stage and control stage has been is provided.

Chapter 3

BATTERY CHARGER MODELLING

In this chapter, a discrete-time model is derived for the battery charger circuit. In particular, a discrete-time recurrence of each inductor current, the DC-link voltage and battery voltage are obtained. These recurrences will be applied afterwards in the design of the feedback control loops detailed in Chapter 4.

3.1 Steady-state averaged model

The two-cascaded stages of the battery charger after the grid rectification are depicted in Fig. 3.1. As it can be seen, the input voltage corresponds to the absolute value of the grid AC voltage due to the rectification. First stage is based on three parallel boost converters which are connected to the DC-link capacitor and the second stage. The second stage consists of three parallel buck converters that are connected to the battery. Note that the current absorbed by the second stage is defined as $i_o(t)$.

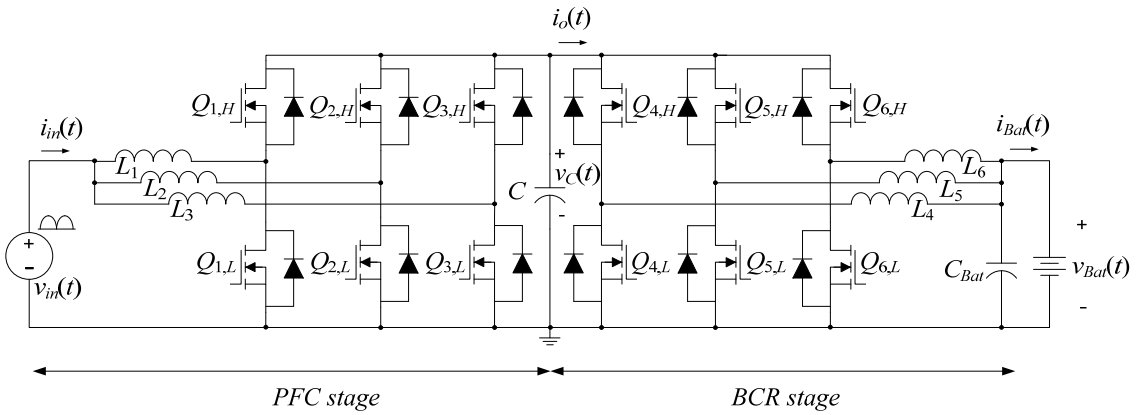


Fig. 3.1. General view of the two-cascaded stages of the battery charger.

Ideally, in G2V operation all the absorbed power by the first stage from the grid (P_{in}) is transmitted to the second stage (P_o) to be absorbed again and be transferred to the battery (P_{Bat}). Hence, it is possible to define the following power expressions

$$P_{in} = V_{in} I_{in} \tag{3.1}$$

$$P_o = V_C I_o \tag{3.2}$$

$$P_{Bat} = V_{Bat} I_{Bat} \tag{3.3}$$

where V_{in}, I_{in}, V_c, I_o, V_{Bat} and I_{Bat} stand for the steady-state averaged values of input, DC-link and battery variables. Note that in V2G operation, voltage signs do not change their polarity, but currents $i_{in}(t)$, $i_o(t)$ and $i_{Bat}(t)$ flow on the opposite direction that they are defined in Fig. 3.1. For that reason, P_{in}, P_o and P_{Bat} become negative in V2G operation.

Firstly, the digital controller will be designed to impose an LFR behaviour [77] on the PFC stage in order to achieve a proportional correspondence between input voltage $v_{in}(t)$ and input current $i_{in}(t)$ as defined in (3.4) and, in consequence, a high power factor.

$$I_{in} = \frac{V_{in}}{r} \tag{3.4}$$

An LFR consists in a two-port structure whose input current is proportional to the input voltage and all the power absorbed by the input port P_{in} is ideally transmitted to the output port. For that reason, LFRs are considered a type of POPI systems, because it is supposed that there is no power loss during the power transmission. The LFR model is depicted in Fig. 3.2.

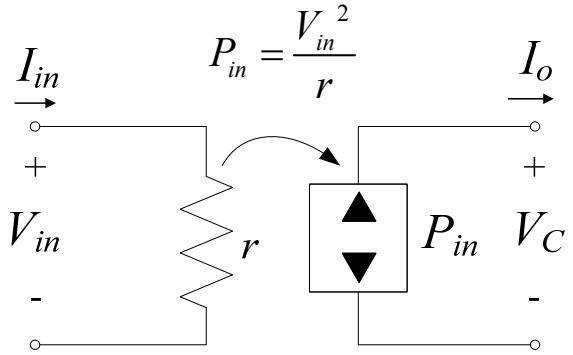


Fig. 3.2. LFR model.

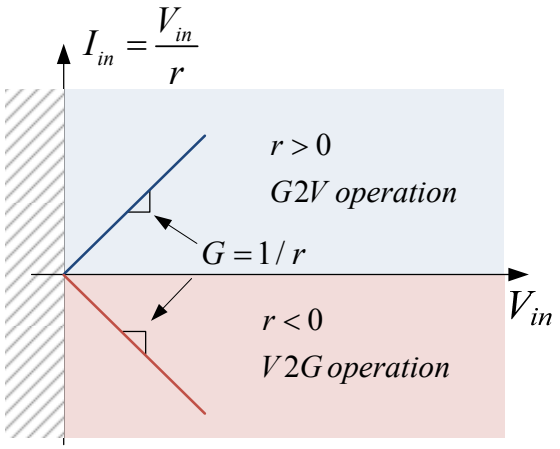


Fig. 3.3. Proportionality between input current I_{in} and input voltage V_{in}.

Parameter r of an LFR represents the input resistive impedance exhibited by the circuit in steady-state. It is also possible to define r as $1/G$, where G represents the conductance of the LFR.

It is important to highlight that for a bidirectional system, the direction of the power flow depends on the sign of parameter r. As it can be seen in Fig. 3.3, for $r > 0$ the battery charger is going to operate in G2V mode while for $r<0$ it is going to operate in V2G mode.

The objective is to design the digital controller in order to impose the same proportional relation on each cell so that the total input current is shared equally through the different boost converters. Therefore, it is also possible to represent each cell of the PFC stage as an individual LFR that transmits its absorbed power to the output as it can be observed in Fig. 3.4. Hence, the total input resistive impedance r corresponds to the equivalent resistance value of the parallel resistors r_1, r_2 and r_3 while the total output power P_o results in the sum of the three power sources P_1, P_2 and P_3. In order to achieve a proper current distribution through the parallel cells, they need to exhibit the same emulated input resistance, i.e. $r_1=r_2=r_3$, and, in consequence, $r=r_j/3$ and $P_1=P_2=P_3= P_o/3$. This allows defining the conductance of a single cell as $g=1/r_j=G/3$ and it will be used to calculate the inductor current reference of the three boost converters.

$$r = \frac{r_1 \cdot r_2 \cdot r_3}{r_1 \cdot r_2 + r_2 \cdot r_3 + r_1 \cdot r_3} \tag{3.5}$$

$$P_o = P_1 + P_2 + P_3 \tag{3.6}$$

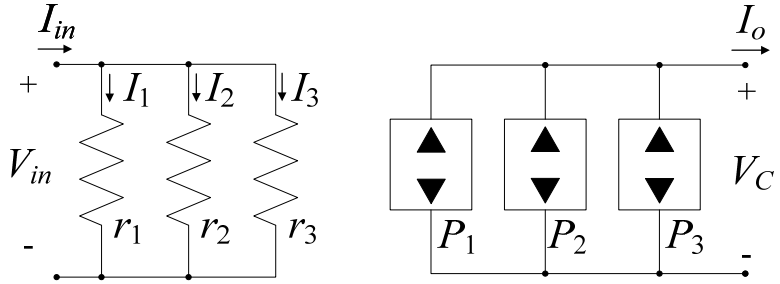


Fig. 3.4. Equivalent representation of the PFC stage based on three parallel connected LFRs.

3.2 Power converters modelling

3.2.1 Continuous-time modelling

Next step is to model each cell of both stages separately. It must be borne in mind that the DC-link capacitor receives the current from the three parallel converters and it has to deliver current $i_o(t)$ to supply the second stage. From the point of view of the PFC stage, the second stage behaves as a constant power load (CPL) (see Fig. 3.5.a) since the product of the battery current and the battery voltage is meant to vary very slowly with respect the PFC stage dynamics

[106]. Note also that for V2G operation mode, currents $i_o(t)$ and $i_{Lj}(t)$ will be both negative and the BCR will behave as a constant power source (CPS) as depicted in Fig. 3.5.b.

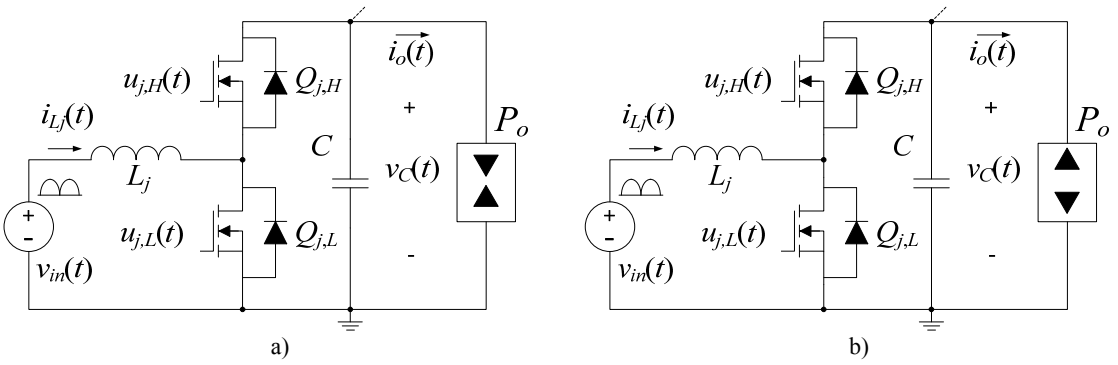


Fig. 3.5. Continuous-time modelling of the PFC stage cells. Boost converter connected to a a) CPL for G2V operation mode, b) CPS for V2G operation mode.

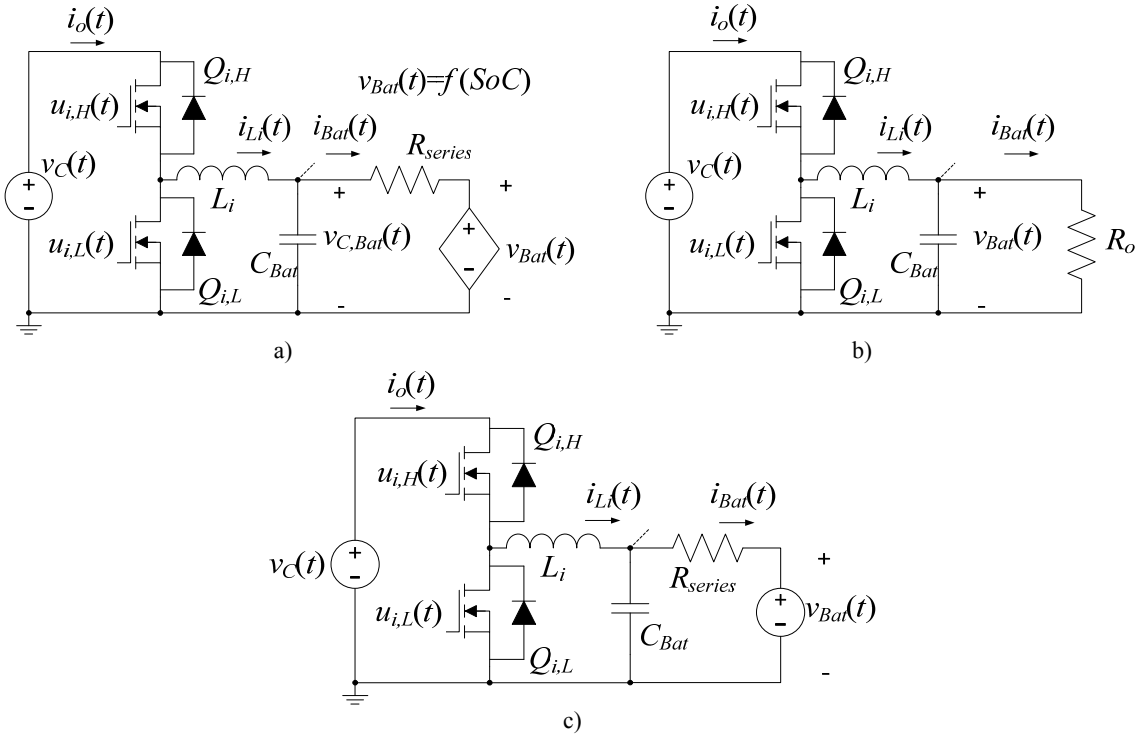


Fig. 3.6. Continuous-time modelling of the BCR stage cells. Buck converter connected to a b) Thévenin's simplified model of a battery, c) a resistive load, d) a DC voltage source for V2G operation mode.

Besides, from the point of view of the BCR stage, the DC-link capacitor acts like a DC voltage source with one harmonic at twice the line frequency due to the pre-regulation operation of the PFC stage (see Fig. 3.6.a-c). In fact, DC-link voltage has not been considered as a state variable for the BCR stage cells because it is regulated by the PFC stage. Regarding the battery modelling, one option is to use a Thévenin's simplified model [107] as depicted in Fig. 3.6.a. This model consists of a resistor with a very low resistance value connected in series to a controlled voltage source that depends on the SoC of the battery. The SoC function is a very specific characteristic for each battery and it does not only depend on the battery voltage. In

fact, simulation and experimental results for G2V operation mode will be carried out by means of a resistive electronic load instead of using a real battery and, for that reason, the battery has been modelled as a resistor as in Fig. 3.6.b. Finally, a DC voltage source and a very low value resistance connected in series will be employed for modelling the battery during V2G operation mode as illustrated in Fig. 3.6.c.

Then, assuming that all the battery charger cells operate at a constant switching frequency and in CCM, it is possible to define two conduction topologies for each converter depending on their corresponding control signal $u_k(t)$. As it can be seen in Fig. 3.7, the converter will be in ON topology if $u_k(t)$=1 or in OFF topology if $u_k(t)$=0. In the particular case of boost converters, signal $u_j(t)$=1 corresponds to the activation of the low-side controlled MOSFET ($u_{j,L}(t)$=1) while for buck converters $u_i(t)$=1 implies activating the high-side controlled MOSFET ($u_{i,H}(t)$=1).

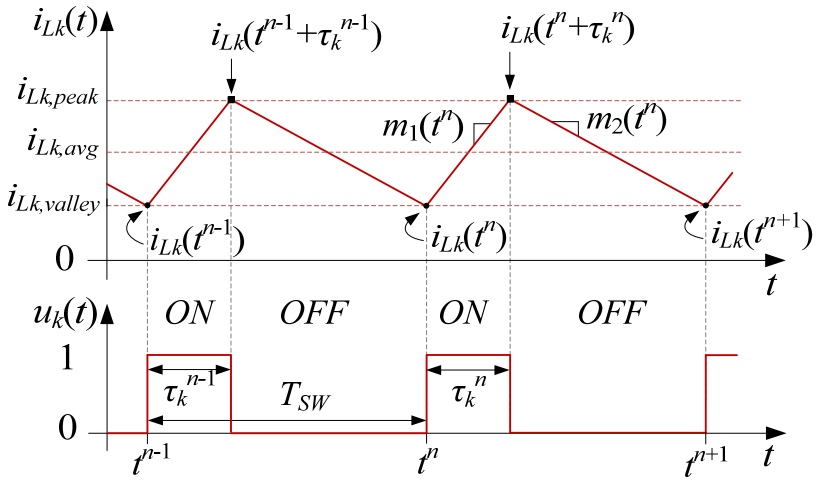


Fig. 3.7. Theoretical behaviour of one cell inductor current.

Note that the ON-state topology starts at the beginning of the n^{th} switching period and its duration is defined by τ_k^n, which stands for the ON conduction time of each cell. As it will be seen in next chapter, ON conduction-time τ_k^n will act as the control action of current-mode controllers. Once τ_k^n is finished, the converter switches into the OFF-state topology for the rest of the switching period. Furthermore, $i_{Lk}(t)$ exhibits a different slope during each conduction topology; during the ON-state topology the slope is equal to $m_1(t)$ while during the OFF-state topology it is equal to $m_2(t)$. Although, the definition of these slopes depends on the type of converter, they are assumed to be constant during a switching period since they depend directly on the converters' input and output voltages, which are assumed to exhibit a slower dynamics with respect inductor currents. The inductance value will be also assumed to be constant.

Hence, the continuous-time dynamics of state variables are described by the following two linear differential equations

$$\dot{x}_k(t) = A_{1,k}x_k(t) + B_{1,k} \qquad t^n < t \le t^n + \tau_k{}^n \tag{3.7}$$

$$\dot{x}_k(t) = A_{2,k}x_k(t) + B_{2,k} \qquad t^n + \tau_k{}^n < t \le t^n + T_{SW} \tag{3.8}$$

where $x_k(t)$ is the vector of the state variables, symbol ($\dot{}$) represents the time derivative operation and t^n stands for the moment at which the n^{th} switching period is started, so that, $t^{n+1} = t^n + T_{SW}$. Both equations (3.7) and (3.8) can be combined to describe the averaged state-space model [108] of the system as follows

$$\dot{x}_k(t) = A_{2,k}x_k(t) + \left[\left(A_{1,k} - A_{2,k}\right)x_k(t) + \left(B_{1,k} - B_{2,k}\right)\right]d_k\left(t^n\right) + B_{2,k} \tag{3.9}$$

where $d_k(t^n)$ represents the duty cycle of the n^{th} switching period and it is defined as follows

$$d_k\left(t^n\right) = \frac{\tau_k^n}{T_{SW}}, \quad 0 < d_k\left(t^n\right) < 1 \tag{3.10}$$

It is important to remark that, state vector $x_k(t)$ is different for each stage. In the particular case of the boost cells (k=j), the state vector of each cell is defined as follows

$$x_j(t) = \left[i_{Lj}(t) \;\; v_C(t)\right]^T \tag{3.11}$$

where ^{T} indicates the transpose of the vector.

Considering that both topologies are ideal lossless systems, that control signal $u_j(t)$ corresponds to the low-side MOSFETs (see Fig. 3.10), the three cells are equally balanced ($i_{L1}(t)$=$i_{L2}(t)$=$i_{L3}(t)$) and their ON conduction times are also the same ($\tau_1{}^n$= $\tau_2{}^n$= $\tau_3{}^n$), state matrices $A_{1,j}$, $A_{2,j}$, $B_{1,j}$ and $B_{2,j}$ are the following

$$A_{1,j} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \qquad A_{2,j} = \begin{bmatrix} 0 & -\frac{1}{L_j} \\ \frac{3}{C} & 0 \end{bmatrix} \qquad B_{1,j} = B_{2,j} = \begin{bmatrix} \frac{v_{in}(t)}{L_j} \\ \frac{-i_o(t)}{C} \end{bmatrix} \tag{3.12}$$

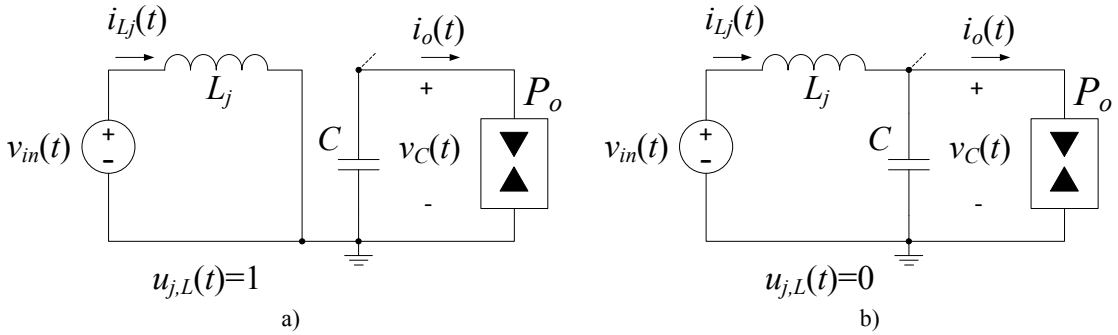


Fig. 3.8. Ideal boost converter conduction topologies. a) On-state for $u_{j,L}(t)$=1. b) Off-state for $u_{j,L}(t)$=0.

On the other hand, for the buck cells case (k=i), two operation modes have to be considered: G2V and V2G. In the particular case of G2V operation, each cell exhibits two state variables,

i.e. inductor current and battery voltage. Therefore their corresponding state vectors are defined as follows

$$x_i(t) = \left[i_{Li}(t) \;\; v_{Bat}(t) \right]^T \tag{3.13}$$

Considering that both topologies are ideal lossless systems, that control signal $u_i(t)$ corresponds to the high-side MOSFETs (see Fig. 3.10.), the three cells are equally balanced ($i_{L4}(t)=i_{L5}(t)=i_{L6}(t)$) and their ON-state conduction times τ_i^n are also the same ($\tau_4^n = \tau_5^n = \tau_6^n$), state matrices $A_{1,i}$, $A_{2,i}$, $B_{1,i}$ and $B_{2,i}$ are the following

$$A_{1,i} = A_{2,i} = \begin{bmatrix} 0 & -\dfrac{1}{L_i} \\ \dfrac{3}{C_{Bat}} & -\dfrac{1}{R_o C_{Bat}} \end{bmatrix} \qquad B_{1,i} = \begin{bmatrix} \dfrac{v_C(t)}{L_i} \\ 0 \end{bmatrix} \qquad B_{2,i} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{3.14}$$

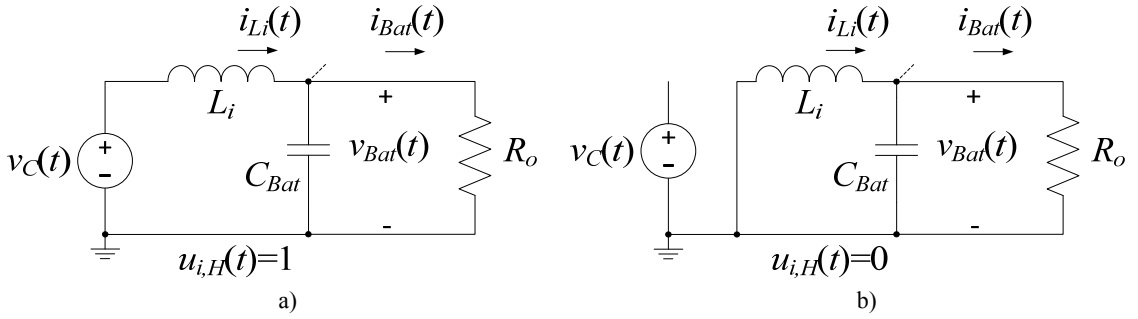


Fig. 3.9. Ideal buck converter conduction topologies during G2V operation. a) On-state for $u_{i,H}(t)=1$, b) Off-state for $u_{i,H}(t)=0$.

However, in V2G operation, the battery voltage cannot be considered as a state variable because it transforms into a superfluous elements in the circuit and, for that reason, the system's order is reduced to only one state variable for each cell as defined in (3.15). Assuming the same conditions as before and that the resistance of R_{series} can be neglected due to its low value, their dynamics comes defined by scalar functions (3.16) which can be deduced from Fig. 3.10.

$$x_i(t) = i_{Li}(t) \tag{3.15}$$

$$A_{1,i} = A_{2,i} = 0 \qquad B_{1,i} = \frac{v_C(t) - v_{Bat}(t)}{L_i} \qquad B_{2,i} = -\frac{v_{Bat}(t)}{L_i} \tag{3.16}$$

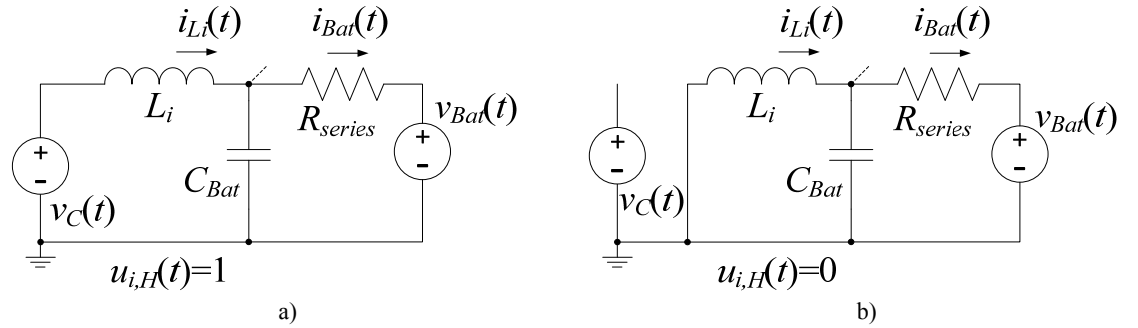


Fig. 3.10. Ideal buck converter conduction topologies during V2G operation. a) On-state for $u_{i,H}(t)=1$, b) Off-state for $u_{i,H}(t)=0$.

3.2.2 Discrete-time modelling

A discrete-time model of the switching converter is first derived to characterise the dynamic behaviour of the power stage since this model will be used later on the controllers' design.

Firstly, the discrete-time recurrence of inductor currents is obtained. It can be easily deduced from Fig. 3.7 that the theoretical value of inductor current $i_{Lk}(t)$ at $t=t^{n+1}$ can be obtained by the combination of the following two equations:

$$i_{Lk}\left(t^n+\tau_k{}^n\right)=i_{Lk}\left(t^n\right)+m_1\left(t^n\right)\tau_k{}^n \tag{3.17}$$

$$i_{Lk}\left(t^{n+1}\right)=i_{Lk}\left(t^n+\tau_k{}^n\right)+m_2\left(t^n\right)\left(T_{SW}-\tau_k{}^n\right) \tag{3.18}$$

Variables $i_{Lk}(t^n)$, $i_{Lk}(t^{n+1})$, $m_1(t^n)$ and $m_2(t^n)$ are redefined as $i_{Lk}{}^n$, $i_{Lk}{}^{n+1}$, $m_1{}^n$ and $m_2{}^n$ respectively in order to simplify the notation. Substituting (3.17) into (3.18) leads to

$$i_{Lk}{}^{n+1}=i_{Lk}{}^n+\left(m_1{}^n-m_2{}^n\right)\tau_k{}^n+m_2{}^nT_{SW} \tag{3.19}$$

Note that in steady-state, i.e. $i_{Lk}{}^{n+1}=i_{Lk}{}^n$, the duration of the ON-state conduction time has the following expression.

$$\tau_{k,SS}{}^n=\left(\frac{m_2{}^n}{m_2{}^n-m_1{}^n}\right)T_{SW} \tag{3.20}$$

Hence, the average and peak values of inductor current $i_{Lk}(t)$ during the n^{th} switching period can be represented as a function with respect its respective valley current value as follows.

$$i_{Lk,avg}{}^n=i_{Lk}{}^n+m_1{}^n\frac{\tau_{k,SS}{}^n}{2} \tag{3.21}$$

$$i_{Lk,peak}{}^n=i_{Lk}{}^n+m_1{}^n\tau_{k,SS}{}^n \tag{3.22}$$

Both previous expressions will be used when designing current-mode controllers. In particular, expression (3.21) is used later to define the discrete-time recurrence of the voltage-type state variables, which can be obtained by applying the forward-Euler approximation of the continuous-time model defined in (3.9) [109]. Since the recurrence for each voltage-type state variable is different for each converter, the following part is focused on obtaining the specific discrete-time state-variables recurrences for both types of cells, i.e. boost and buck converters.

3.2.2.1 Boost-type cells discrete-time model

For the boost converter case, slopes $m_1{}^n$ and $m_2{}^n$ come defined as follows.

$$m_1{}^n=\frac{v_{in}{}^n}{L_j} \tag{3.23}$$

$$m_2{}^n=\frac{v_{in}{}^n-v_C{}^n}{L_j} \tag{3.24}$$

where $v_{in}^{\ n}$ and $v_C^{\ n}$ stand for the sampled values of $v_{in}(t)$ and $v_C(t)$ at the beginning of the n^{th} switching period. In consequence, it can be demonstrated that the inductor current recurrence has the following form.

$$i_{Lj}^{\ n+1} = i_{Lj}^{\ n} + \left(\frac{v_C^{\ n}}{L_j}\right)\tau_j^{\ n} + \left(\frac{v_{in}^{\ n} - v_C^{\ n}}{L_j}\right)T_{SW} \tag{3.25}$$

Hence, the steady-state ON conduction time $\tau_{j,SS}^{\ n}$ is

$$\tau_{j,SS}^{\ n} = \left(1 - \frac{v_{in}^{\ n}}{v_C^{\ n}}\right)T_{SW} \tag{3.26}$$

In order to satisfy conditions stated in (3.10), it is necessary to satisfy the following two conditions.

$$\frac{v_{in}^{\ n}}{v_C^{\ n}} > 0 \tag{3.27}$$

$$v_{in}^{\ n} < v_C^{\ n} \tag{3.28}$$

Condition (3.27) is always fulfilled since both $v_{in}^{\ n}$ and $v_C^{\ n}$ are positive while condition (3.28) is fulfilled for boost converters under normal operation conditions. Furthermore, inductor current $i_{Lj,avg}^{\ n}$ and $i_{Lj,peak}^{\ n}$ are defined as follows.

$$i_{Lj,avg}^{\ n} = i_{Lj}^{\ n} + \frac{v_{in}^{\ n}}{2L_j}\left(1 - \frac{v_{in}^{\ n}}{v_C^{\ n}}\right)T_{SW} \tag{3.29}$$

$$i_{Lj,peak}^{\ n} = i_{Lj}^{\ n} + \frac{v_{in}^{\ n}}{L_j}\left(1 - \frac{v_{in}^{\ n}}{v_C^{\ n}}\right)T_{SW} \tag{3.30}$$

Finally, the application of Euler's method on the average state-space description of continuous-time DC-link capacitor voltage results in the following discrete-time recurrence.

$$v_C^{\ n+1} = v_C^{\ n} - \frac{3i_{Lj,avg}^{\ n}}{C}\tau_j^{\ n} + \left(\frac{3i_{Lj,avg}^{\ n} - i_o^{\ n}}{C}\right)T_{SW} \tag{3.31}$$

where $i_o^{\ n}$ stands for the theoretical value of i_o(t) at the beginning of the n^{th} switching period and its value is expected to be

$$i_o^{\ n} = \frac{v_{Bat}^{\ n} i_{Bat}^{\ n}}{v_C^{\ n}} \tag{3.32}$$

where $v_{Bat}^{\ n}$ stands for the sampled value of $v_{Bat}(t)$ at the beginning of the n^{th} switching period. However, $i_{Bat}(t)$ is not being measured, so that $i_{Bat}^{\ n}$ is supposed to be three times the average value of buck inductor currents $i_{Li,avg}^{\ n}$ during the n^{th} period. Therefore, it is possible to rewrite $v_C^{\ n+1}$ as follows.

$$v_C^{n+1} = v_C^n + \left(\frac{3i_{Lj,avg}^n}{C}\right)\left(T_{SW} - \tau_j^n\right) - \left(\frac{3v_{Bat}^n i_{Li,avg}^n}{Cv_C^n}\right)T_{SW} \tag{3.33}$$

3.2.2.2 Buck-type cells discrete-time model

For the buck converter cells, slopes m_1^n and m_2^n come defined as follows.

$$m_1^n = \frac{v_C^n - v_{Bat}^n}{L_i} \tag{3.34}$$

$$m_2^n = -\frac{v_{Bat}^n}{L_i} \tag{3.35}$$

where v_{Bat}^n stands for the sampled value of $v_{Bat}(t)$ at the beginning of the n^{th} switching period. In consequence, it can be demonstrated that

$$i_{Li}^{n+1} = i_{Li}^n + \left(\frac{v_C^n}{L_i}\right)\tau_i^n - \left(\frac{v_{Bat}^n}{L_i}\right)T_{SW} \tag{3.36}$$

Hence, the steady-state ON conduction time $\tau_{i,SS}^n$ is

$$\tau_{i,SS}^n = \left(\frac{v_{Bat}^n}{v_C^n}\right)T_{SW} \tag{3.37}$$

In order to comply with condition (3.10), it is necessary to satisfy the following two conditions.

$$\frac{v_{Bat}^n}{v_C^n} > 0 \tag{3.38}$$

$$v_{Bat}^n < v_C^n \tag{3.39}$$

Condition (3.38) is always fulfilled since both v_{Bat}^n and v_C^n are always positive and condition (3.39) is fulfilled for any buck converter under normal operation conditions. Moreover, inductor current values $i_{Li,avg}^n$ and $i_{Li,peak}^n$ are defined as follows.

$$i_{Li,avg}^n = i_{Li}^n + \left(\frac{v_C^n - v_{Bat}^n}{2L_i}\right)\left(\frac{v_{Bat}^n}{v_C^n}\right)T_{SW} \tag{3.40}$$

$$i_{Li,peak}^n = i_{Li}^n + \left(\frac{v_C^n - v_{Bat}^n}{L_i}\right)\left(\frac{v_{Bat}^n}{v_C^n}\right)T_{SW} \tag{3.41}$$

Finally, it can be demonstrated that the discrete-time recurrence of the average battery voltage considering a resistive load is given by the following expression.

$$v_{Bat}^{n+1} = v_{Bat}^n\left(1 - \frac{T_{SW}}{R_o C_{Bat}}\right) + \left(\frac{3i_{Li,avg}^n}{C_{Bat}}\right)T_{SW} \tag{3.42}$$

3.2.3 Summary

The following table aims to summarise the discrete-time modelling equations of each converter.

Variable	Boost (*k=j*)	Buck (*k=i*)
$m_1^{\,n}$	$\frac{v_{in}^{\,n}}{L_j}$	$\frac{v_C^{\,n}-v_{Bat}^{\,n}}{L_i}$
$m_2^{\,n}$	$\frac{v_{in}^{\,n}-v_C^{\,n}}{L_j}$	$-\frac{v_{Bat}^{\,n}}{L_i}$
$i_{Lk}^{\,n+1}$	$i_{Lj}^{\,n}+\left(\frac{v_C^{\,n}}{L_j}\right)\tau_j^{\,n}+\left(\frac{v_{in}^{\,n}-v_C^{\,n}}{L_j}\right)T_{SW}$	$i_{Li}^{\,n}+\left(\frac{v_C^{\,n}}{L_i}\right)\tau_i^{\,n}-\left(\frac{v_{Bat}^{\,n}}{L_i}\right)T_{SW}$
$\tau_{k,SS}^{\,n}$	$\left(1-\frac{v_{in}^{\,n}}{v_C^{\,n}}\right)T_{SW}$	$\left(\frac{v_{Bat}^{\,n}}{v_C^{\,n}}\right)T_{SW}$
$i_{Lk,avg}^{\,n}$	$i_{Lj}^{\,n}+\frac{v_{in}^{\,n}}{2L_j}\left(1-\frac{v_{in}^{\,n}}{v_C^{\,n}}\right)T_{SW}$	$i_{Li}^{\,n}+\left(\frac{v_C^{\,n}-v_{Bat}^{\,n}}{2L_i}\right)\left(\frac{v_{Bat}^{\,n}}{v_C^{\,n}}\right)T_{SW}$
$i_{Lk,peak}^{\,n}$	$i_{Lj}^{\,n}+\frac{v_{in}^{\,n}}{L_j}\left(1-\frac{v_{in}^{\,n}}{v_C^{\,n}}\right)T_{SW}$	$i_{Li}^{\,n}+\left(\frac{v_C^{\,n}-v_{Bat}^{\,n}}{L_i}\right)\left(\frac{v_{Bat}^{\,n}}{v_C^{\,n}}\right)T_{SW}$
$v_C^{\,n+1}$	$v_C^{\,n}+\left(\frac{3i_{Lj,avg}^{\,n}}{C}\right)\left(T_{SW}-\tau_j^{\,n}\right)-\left(\frac{3v_{Bat}^{\,n}i_{Li,avg}^{\,n}}{Cv_C^{\,n}}\right)T_{SW}$	-
$v_{Bat}^{\,n+1}$	-	$v_{Bat}^{\,n}\left(1-\frac{T_{SW}}{R_oC_{Bat}}\right)+\left(\frac{3i_{Li,avg}^{\,n}}{C_{Bat}}\right)T_{SW}$

Table 3.1. Discrete-time system modelling equations.

3.3 Conclusions

One of the most important conclusions of the chapter is that the PFC stage has to behave as an LFR in order to achieve a high PF. In fact, the three boost converters of the first stage are expected to behave as three equal LFRs in order to ensure that the total input current is equally shared through the three converters.

Moreover, a suitable discrete-time model of the battery charger has been obtained in this chapter, considering the following signals as state variables: each inductor current, the DC-link voltage and the battery voltage, taking into account a resistive load in the particular case of this latter. The derived recurrences will allow a direct digital control design of the different controllers in the next chapter.

However, it is important to highlight that these recurrences have been obtained taking into account different considerations. In this sense, one assumption is that the BCR stage behaves as

a CPL or a CPS (depending on the direction of the power flow) with respect the PFC stage because the battery voltage and battery current are meant to exhibit a very slow dynamics with respect the PFC state variables. Another assumption is that the DC-link capacitor behaves as a voltage source with respect the BCR stage with independence of the direction of the power flow because the DC-link voltage is regulated by the PFC stage at any time. Moreover, the battery has been modelled as a resistive load for the G2V operation mode, and as a voltage source for the V2G operation mode. Another important assumption is that all cells have been considered ideal loss-less systems which operate in CCM.

Chapter 4

DIGITAL CONTROLLER DESIGN

This chapter presents the design of the digital controllers and it specially focuses on the design of the inductor current-mode controllers by means of the application of the discrete-time SMC theory. The design of the outer control loops for the DC-link and battery voltages are also included. These voltage controllers will be derived from the ideal discrete-time dynamics of the system assuming that inductor currents are in discrete-time sliding-mode regime.

The objectives of the PFC controller are to impose an LFR behaviour on the PFC stage and to regulate the DC-link voltage at the desired level, whereas the BCR controller is meant to impose the CC or CV operation mode on the BCR stage depending on the battery voltage.

This chapter also describes how the digital control has been organized in order to allow its implementation in a single DSC, including a detailed description of the proposed control execution sequence. The interleaved control signals generation and the computation-time of the most important parts of the control algorithm are illustrated in the end of the chapter to demonstrate the feasibility of the proposed control sequence.

4.1 Digital controller overview

Having defined the battery charger circuit and obtained a discrete-time model of each state variable of the system, it is possible to start the digital control design. The digital control algorithm has to regulate in total eight variables: six inductor currents, the DC-link voltage and the battery voltage. As it can be observed in Fig. 4.1, the three inductor currents of the PFC stage and the DC-link voltage are regulated by the PFC controller, while the three inductor currents of the BCR stage and the battery voltage are managed by the BCR controller.

The PFC controller has two main tasks. On one hand, it has to impose an LFR on the first stage in order to allow the achievement of a high PF. On the other hand, it has to regulate the DC-link voltage at the desired voltage. As it can be seen in Fig. 4.1, the DC-link voltage regulation loop calculates the necessary conductance G that the PFC stage has to exhibit at the input port. It is important to remind that the input conductance is directly related to the absorbed input power, i.e. a higher conductance implies that a higher power absorbed from the grid. Moreover, while a positive conductance G means that the battery charger works in G2V operation, a negative

conductance implies the injection of current into the grid (V2G operation). As it can be seen, the current reference of the whole PFC stage is given by the product between conductance *G* and the sampled information of the rectified input voltage. Then, it can be deduced that the current reference for each inductor current-mode controller has to be equal to one third of the total current reference in order to share it equally among the three inductors of the PFC stage.

The main task of the BCR controller when the battery is being charged (G2V operation) is to allow the CC or CV operation modes depending on the battery voltage. While the battery voltage is lower than the nominal voltage, the system works in CC operation mode and a constant current must be delivered to the battery. This can be achieved by saturating the battery current reference at the desired maximum battery current. In contrast, once the battery achieves its nominal voltage, the controller has to start regulating the battery voltage by means of the progressive reduction of the battery current reference.

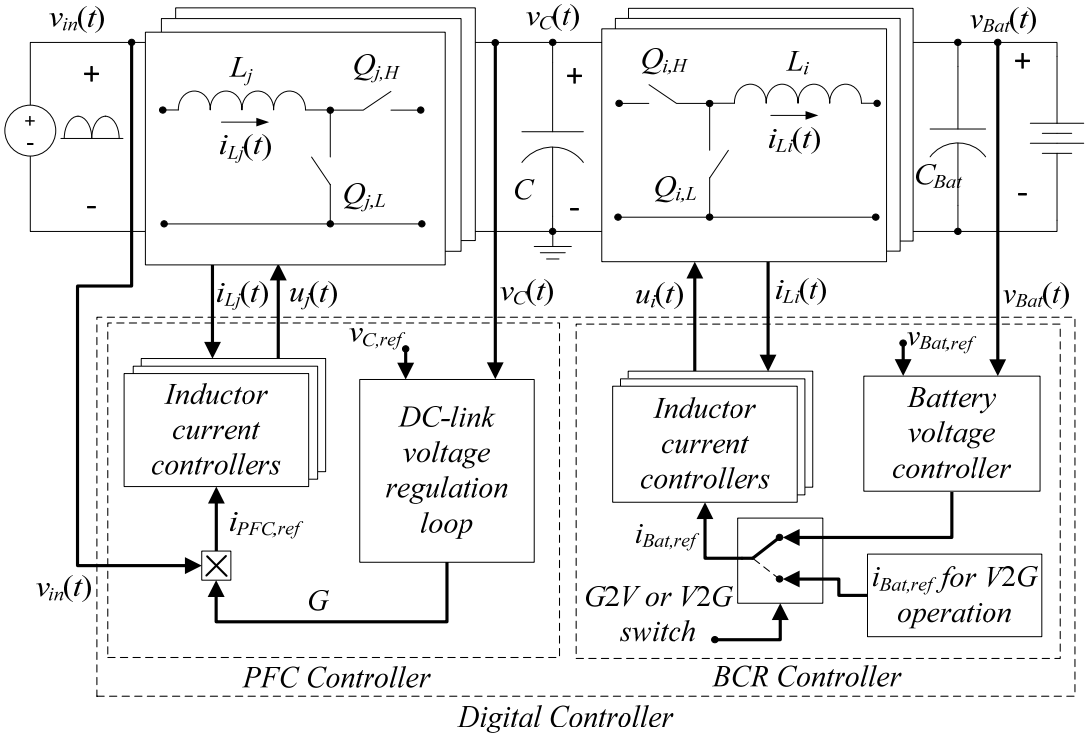


Fig. 4.1. Simplified overview of both digitally controlled stages of the battery charger.

When the system works in V2G operation, the battery current reference should be provided externally from a higher level system. However, in this thesis a programmed battery current reference will be considered. Independently from the direction of the power flow, the current reference of inductor current-mode controllers of the BCR stage has to be one third of the total battery current in order to share the total current equally among the three buck converters.

A more detailed diagram of the whole control algorithm is depicted in Fig. 4.2, which will be implemented in a single TMS320F28335 DSC from TEXAS INSTRUMENTS. As it can be observed, nine different analogue signals, which come from the sensing signals conditioning circuit, are sampled by the ADC of the controller. The analogue-to-digital (AD) conversion of the different sensing signals has to be sequenced in order to use the single ADC that the employed DSC incorporates. Once the samples are obtained, they are introduced into a signal rebuilding algorithm in order to calculate the corresponding value of the actual power stage variables.

The PFC controller part consists of the three discrete-time SM-based inductor current-mode controllers $d_j^n(\tau_j^n)$, the DC-link voltage regulator $G_1(z)$ and a Notch filter $N(z)$, which has been introduced to improve the performance of the PFC stage with regard the quality of the absorbed power from the grid. As it can be observed, the error between the DC-link voltage reference and the sampled DC-link voltage is introduced to compensator $G_1(z)$ which is based on a discrete-time PI controller. Then, the output of this PI controller is filtered by filter $N(z)$ which will be tuned at 100 Hz to remove the oscillations at twice the line frequency that come from the PI regulator due to the DC-link voltage ripple. As commented previously, the output of the DC-link voltage regulation loop is G^n, which stands for the computed conductance of the whole PFC stage at the input terminals of the battery charger, while the conductance of a single PFC cell g^n is calculated as one third of G^n. To impose an LFR behaviour on each cell it is necessary to compute the inductor current reference $i_{Lj,ref}{}^n$ as the multiplication of the rectified input voltage sample $v_{in}{}^n$ and g^n.

$$i_{Lj,ref}{}^n = v_{in}{}^n g^n \tag{4.1}$$

The resulting PFC inductor current reference is limited afterwards for safety reasons. The discrete-time SM-based inductor mode-controllers $d_j^n(\tau_j^n)$ of the PFC controller calculate the required ON-state time that ensures a proper current reference tracking of $i_{Lj,ref}{}^n$ by the corresponding controlled inductor current. Once the required control action is calculated, the resulting duty cycles are sent to the digital PWM (DPWM) modules to generate control signals $u_j(t)$ accordingly.

Besides, the BCR controller is composed by the three discrete-time SM-based inductor current-mode controllers $d_i^n(\tau_i^n)$ and the battery voltage controller $G_2(z)$. As it can be seen, the battery current reference $i_{Bat,ref}{}^n$ is selected depending on the direction of the power flow (defined by P_{dir}). If the battery charger works in G2V operation, battery current reference is computed by $G_2(z)$, whereas a programmed battery current reference ($i_{Bat2Grid,ref}$) is used for V2G operation to simulate the power demand that would come from an external and higher level system.

Note that the output of the battery voltage controller $G_2(z)$ has been saturated. This has been done in order to limit the battery current reference at the level of current that has to be delivered to the battery in CC operation mode, i.e. while the output voltage has not reached the nominal voltage $v_{Bat,ref}$. Once $v_{Bat,ref}$ is reached, battery current reference will be decreased accordingly to maintain the nominal voltage of the battery. Inductor current reference $i_{Li,ref}^{n}$ of the BCR stage cells is computed as one third of the battery current reference and introduced to the inductor current controllers $d_i^n(\tau_i^n)$. As well as for controllers $d_j^n(\tau_j^n)$, the BCR inductor current controllers calculate the control action to ensure a correct inductor current tracking of reference $i_{Li,ref}^{n}$. Afterwards, the duty cycles are transmitted to the corresponding DPWM modules to generate control signals $u_i(t)$ accordingly.

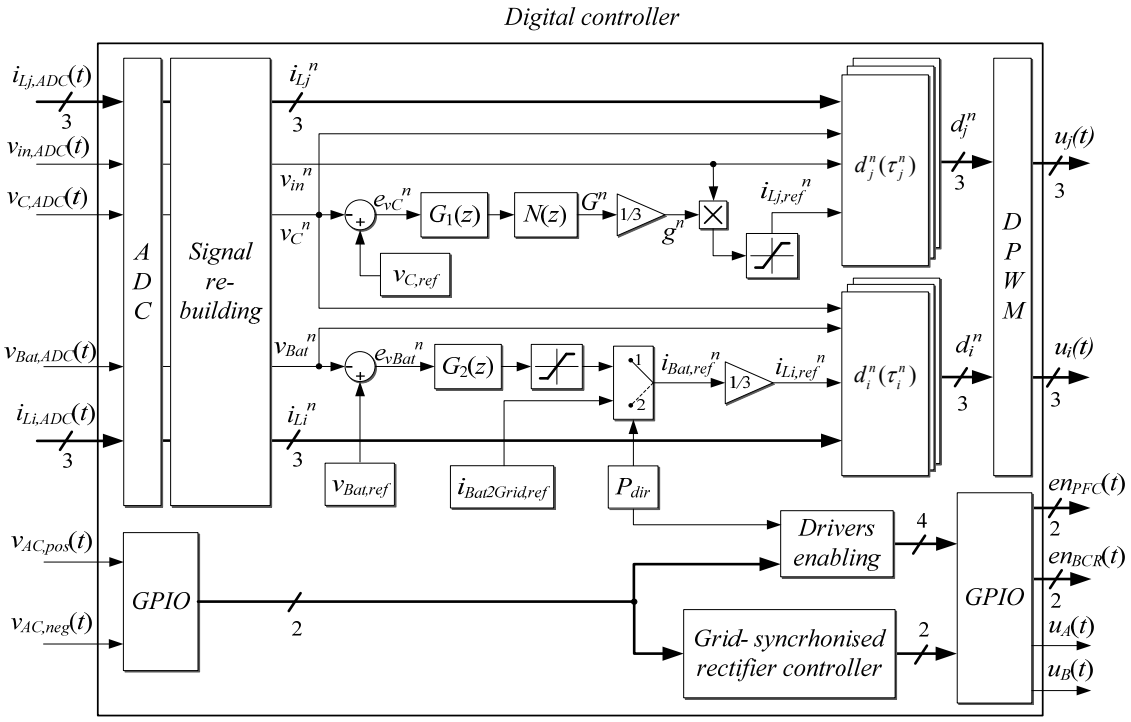


Fig. 4.2. Block diagram of the digital controller.

One interesting detail is that all the DPWM modules of the DSC need to be employed because this particular DSC has in total six different DPWM modules. Trailing-edge modulation has been selected to generate signals $u_k(t)$ in order to have enough time to sample the corresponding signals, calculate the required ON-state time and apply the result at the current switching period. Therefore, the delay of one switching period, which is commonly introduced in the design of digital controllers, is avoided in this case. The AD sampling sequence has been synchronised with the PWM signals in order to take the samples at the beginning of the switching period. For that reason, inductor current samples i_{Lk}^{n} correspond to the valley value of inductor currents $i_{Lk}(t)$. However, voltage samples v_{in}^{n}, v_C^{n} and v_{Bat}^{n} can be assumed to be equal to their average value since they are expected to exhibit a very low high-frequency voltage ripple.

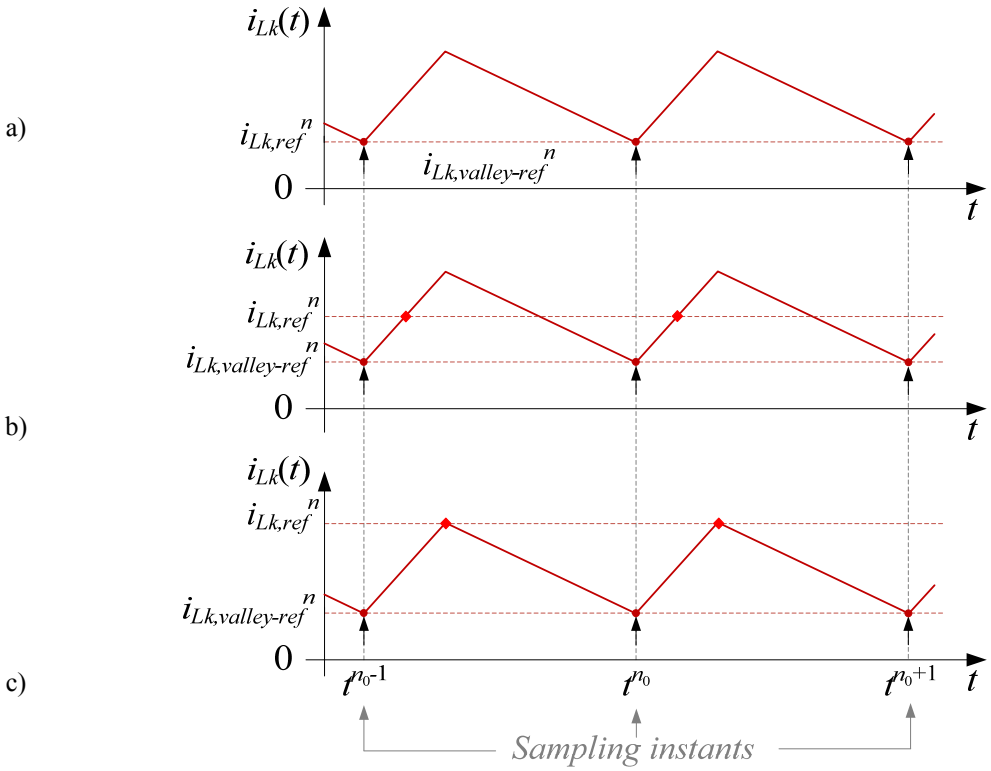


Fig. 4.3. Different types of current-mode control techniques. a) Valley, b) average and c) peak.

4.2 Discrete-time SM-based inductor current-mode controllers

This section is focused on the design of the discrete-time SM-based inductor current-mode controllers by means of the application of the discrete-time SMC theory [76].

4.2.1 Discrete-time sliding control surface

All sliding-mode controllers are based on a switching function (or surface) $s(x(t),t)=0$ which relates the state variables, which are desired to be controlled, with their associated reference. In sliding-mode regime this switching function is characterized by $s(x(t),t)=0$ [76]. In discrete-time, inductor current sample i_{Lk}^{n} is related to its reference $i_{Lk,ref}^{n}$. A noteworthy detail is that in this case, sample i_{Lk}^{n} is only capable to meet the reference at the beginning of the next switching period because reference $i_{Lk,ref}^{n}$ is known at the beginning of the n^{th} switching period. In addition, since the inductor current samples are taken at the valley instant of the inductor current's triangular waveform, the discrete-time sliding control surface is defined as a function of the equivalent valley reference as follows:

$$s_k^{\,n} = i_{Lk,ref-valley}^{\,n-1} - i_{Lk}^{\,n} \tag{4.2}$$

where $i_{Lk,ref\text{-}valley}^{\,n-1}$ stands for the valley reference value of the inductor current during the previous switching period. This reference should be defined according to the desired type of control, i.e. valley, average or peak current-mode control as depicted in Fig. 4.3. As it can be

seen, it is sufficient to adjust $i_{Lk,ref\text{-}valley}{}^{n}$ as $i_{Lk,ref}{}^{n}$ to design a valley current-mode controller. However, the definition of $i_{Lk,ref\text{-}valley}{}^{n}$ for average and peak current-mode controllers is not as direct as for the valley-mode. Table 4.1 summarises how $i_{Lk,ref\text{-}valley}{}^{n}$ has to be defined for each current-mode control technique.

Type of control	$\boldsymbol{i_{Lk,ref\text{-}valley}{}^{n}}$ **definition**
Valley	$i_{Lk,ref}{}^{n}$
Average	$i_{Lk,ref}{}^{n} - m_1{}^{n}\dfrac{\tau_{k,SS}{}^{n}}{2}$
Peak	$i_{Lk,ref}{}^{n} - m_1{}^{n}\tau_{k,SS}{}^{n}$

Table 4.1. Definition of the inductor current valley reference value depending on the desired type of current-mode control technique.

Hence, it is possible to define $i_{Lk,ref\text{-}valley}{}^{n}$ in a compact form for any type of controller as follows

$$i_{Lk,ref-valley}{}^{n} = i_{Lk,ref}{}^{n} - \left(m_1{}^{n}\tau_{k,SS}{}^{n}\right)M \tag{4.3}$$

where

$$M = \begin{cases} 0 & \text{for valley control} \\ \dfrac{1}{2} & \text{for average control} \\ 1 & \text{for peak control} \end{cases} \tag{4.4}$$

Therefore, sliding surface (4.2) can be rewritten as

$$s_k{}^{n} = \left(i_{Lk,ref}{}^{n-1} - \left(m_1{}^{n-1}\tau_{k,SS}{}^{n-1}\right)M\right) - i_{Lk}{}^{n} \tag{4.5}$$

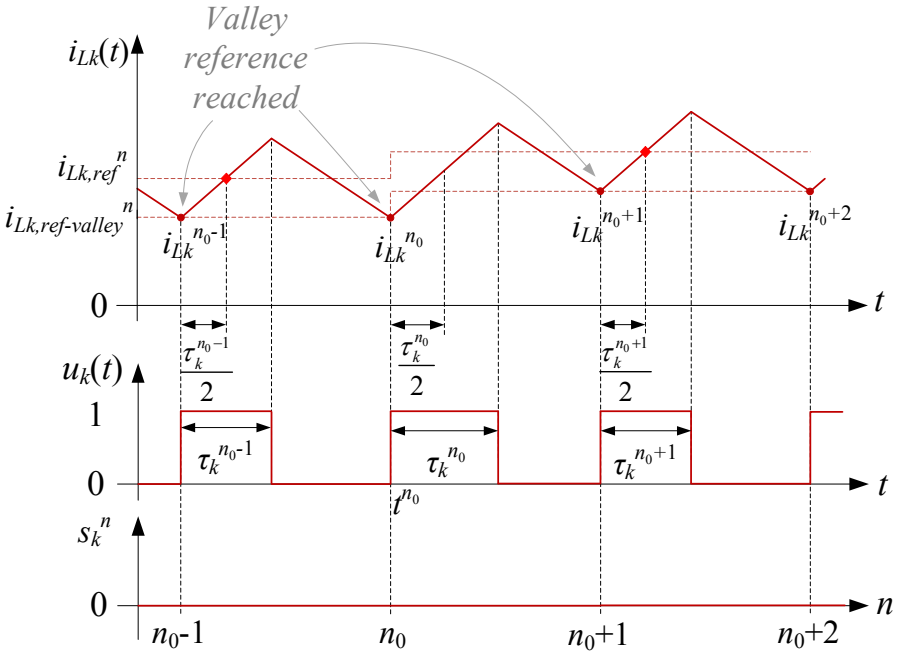


Fig. 4.4. Response example of the discrete-time SM-based current-mode controller in average mode.

Fig. 4.4 depicts how at t^{n0} the corresponding inductor current controller calculates the necessary ON-state time $\tau_k{}^n{}_0$ at the beginning of the switching period in front of a change of the current reference. As it can be seen, the inductor current meets the reference at the beginning of the next period and, for that reason, discrete-time sliding-mode control surface $s_k{}^n$ remains in 0. Thus, the sliding-mode regime is not lost. In fact, the required control action is obtained by applying the sliding-mode existence condition which establishes that the sliding surface $s_k{}^n$ is reached at the beginning of the next switching period [76], i.e.:

$$s_k{}^{n+1} = \left(i_{Lk,ref}{}^n - \left(m_1{}^n \tau_{k,SS}{}^n\right) M\right) - i_{Lk}{}^{n+1} = 0 \tag{4.6}$$

4.2.2 Equivalent control

If the discrete-time dynamics of the inductor current $i_{Lk}{}^{n+1}$ defined by equation (3.19) is substituted in (4.6) leads to

$$s_k{}^{n+1} = \left(i_{Lk,ref}{}^n - \left(m_1{}^n \tau_{k,SS}{}^n\right) M\right) - \left(i_{Lk}{}^n + \left(m_1{}^n - m_2{}^n\right)\tau_k{}^n + m_2{}^n T_{SW}\right) = 0 \tag{4.7}$$

The solution of (4.7) for $\tau_k{}^n$ is defined as the equivalent control $\tau_{eq,k}{}^n$ and it is responsible of keeping the controlled variable on the sliding surface $s(x)$=0.

$$\tau_{eq,k}{}^n = \frac{\left(i_{Lk,ref}{}^n - i_{Lk}{}^n\right) - m_2{}^n T_{SW} - \left(m_1{}^n \tau_{k,SS}{}^n\right) M}{m_1{}^n - m_2{}^n} \tag{4.8}$$

In this sense, Table 4.2 summarises the resulting equivalent control $\tau_{eq,k}{}^n$ for boost and buck converters for valley, average and peak current-mode control. Although it is known that divisions are a very time consuming operation for digital controllers, it is interesting to see that the denominator of all the equivalent control expressions is the same, i.e. $v_C{}^n$. This is very important to reduce the computation time because it allows the controller to calculate $1/\ v_C{}^n$ only once and use the result for all the controllers instead of calculating this division for each controller. Finally, it is also important to highlight that the duration of the ON-state time $\tau_k{}^n$ will be equal to $\tau_{eq,k}{}^n$ in sliding mode regime. Otherwise, $\tau_k{}^n$ has to be theoretically limited as follows to prevent the loss of the constant switching frequency.

$$0 < \tau_k{}^n < T_{SW} \tag{4.9}$$

Note that if $\tau_k{}^n$ was equal to any of both limits 0 or T_{SW}, the system would not switch and the constant switching frequency would be lost. In practice, the minimum applicable ON-state time corresponds to the time it takes to compute $\tau_{eq,k}{}^n$ in each switching period, which will depend on the calculation capabilities of the controller. Finally, duty cycle $d_k{}^n$ is computed as follows.

$$d_k{}^n = \frac{\tau_k^n}{T_{SW}} \tag{4.10}$$

Type of converter	Type of control	$\tau_{eq,k}{}^{n}$
Boost (k=j)	Valley	$\tau_{eq,j}{}^{n} = \dfrac{L_j\left(i_{Lj,ref}{}^{n} - i_{Lj}{}^{n}\right) + T_{SW}\left(v_C{}^{n} - v_{in}{}^{n}\right)}{v_C{}^{n}}$
	Average	$\tau_{eq,j}{}^{n} = \dfrac{L_j\left(i_{Lj,ref}{}^{n} - i_{Lj}{}^{n}\right) + T_{SW}\left(v_C{}^{n} - v_{in}{}^{n}\right)\left(1 - \dfrac{v_{in}{}^{n}}{2v_C{}^{n}}\right)}{v_C{}^{n}}$
	Peak	$\tau_{eq,j}{}^{n} = \dfrac{L_j\left(i_{Lj,ref}{}^{n} - i_{Lj}{}^{n}\right) + T_{SW}\left(v_C{}^{n} - v_{in}{}^{n}\right)^2\left(\dfrac{1}{v_C{}^{n}}\right)}{v_C{}^{n}}$
Buck (k=i)	Valley	$\tau_{eq,i}{}^{n} = \dfrac{L_i\left(i_{Li,ref}{}^{n} - i_{Li}{}^{n}\right) + T_{SW} v_{Bat}{}^{n}}{v_C{}^{n}}$
	Average	$\tau_{eq,i}{}^{n} = \dfrac{L_i\left(i_{Li,ref}{}^{n} - i_{Li}{}^{n}\right) + T_{SW}\left(v_C{}^{n} + v_{Bat}{}^{n}\right)\left(\dfrac{v_{Bat}{}^{n}}{2v_C{}^{n}}\right)}{v_C{}^{n}}$
	Peak	$\tau_{eq,i}{}^{n} = \dfrac{L_i\left(i_{Li,ref}{}^{n} - i_{Li}{}^{n}\right) + T_{SW}\left(v_{Bat}{}^{n}\right)^2\left(\dfrac{1}{v_C{}^{n}}\right)}{v_C{}^{n}}$

Table 4.2. Equivalent control $\tau_{eq,k}{}^{n}$ for boost and buck converters and different types of current-mode control techniques.

4.2.3 Ideal discrete-time dynamics

4.2.3.1 Inductor current ideal discrete-time dynamics

Once inductor currents are in sliding-mode regime, the equivalent control ensures that the controlled variable is kept on the sliding surface, this resulting in a reduction of the system's order. This can be demonstrated by substituting equivalent control (4.8) in the discrete-time dynamics of the inductor current $i_{Lk}{}^{n+1}$ defined in (3.19)

$$i_{Lk}{}^{n+1} = i_{Lk,ref}{}^{n} - m_1{}^{n}\tau_{k,SS}{}^{n}M \tag{4.11}$$

As it can be seen, the previous expression is not a recurrence since the future sample of $i_L{}^{n+1}$ does not depend on any past or current state of the variable. Thus, the system does not present any dynamics and, for that reason, the order of the system has been reduced. Moreover, equation (4.11) coincides with (4.3), so that it can be rewritten as follows.

$$i_{Lk}{}^{n+1} = i_{Lk,ref-valley}{}^{n} \tag{4.12}$$

The previous equation also implies that

$$i_{Lk}{}^{n} = i_{Lk,ref-valley}{}^{n-1} \tag{4.13}$$

or, what it is the same,

$$i_{Lk}{}^{n} = i_{Lk,ref}{}^{n-1} - m_1{}^{n-1}\tau_{k,SS}{}^{n-1}M \tag{4.14}$$

As commented previously, the variation of m_1 and $\tau_{k,SS}$ in a switching period can be neglected. Therefore, it is possible to write

$$i_{Lk}{}^{n} = i_{Lk,ref}{}^{n-1} - m_1{}^{n}\tau_{k,SS}{}^{n}M \tag{4.15}$$

Hence, for average current-mode controllers (M=1/2), expression (4.11) results

$$i_{Lk}{}^{n+1} = i_{Lk,ref}{}^{n} - \frac{m_1{}^{n}\tau_{k,SS}{}^{n}}{2} \tag{4.16}$$

which can be rewritten as follows.

$$i_{Lk}{}^{n+1} + \frac{m_1{}^{n}\tau_{k,SS}{}^{n}}{2} = i_{Lk,ref}{}^{n} \tag{4.17}$$

If we assume that in steady-state

$$i_{Lk,avg}{}^{n+1} = i_{Lk}{}^{n+1} + \frac{m_1{}^{n}\tau_{j,SS}{}^{n}}{2} \tag{4.18}$$

then, it is possible to write

$$i_{Lk,avg}{}^{n+1} = i_{Lk,ref}{}^{n} \tag{4.19}$$

Knowing that in the particular case of the PFC stage (k=j), inductor current reference is forced to be $i_{Lj,ref}{}^{n}$=$v_{in}{}^{n}g^{n}$, the reduced dynamics of inductor currents from the PFC stage results

$$i_{Lj,avg}{}^{n+1} = v_{in}{}^{n}g^{n} \tag{4.20}$$

In consequence, it has been demonstrated that the PFC stage will behave as an LFR due to the application of the discrete-time sliding-mode control technique. In this sense, it is also possible to write

$$i_{Lj,avg}{}^{n} = v_{in}{}^{n-1}g^{n-1} \tag{4.21}$$

If the same procedure is applied on the BCR stage cells, it can be demonstrated that it results

$$i_{Li,avg}{}^{n+1} = \frac{i_{Bat,ref}{}^{n}}{3} \tag{4.22}$$

4.2.3.2 DC-link voltage ideal discrete-time dynamics

The reduced discrete-time dynamics of the DC-link voltage (see equation (3.33)) can be obtained if τ_j^n is substituted by $\tau_{eq,k}$, i_{Lj}^n by its definition in (4.15) and $i_{Lj,avg}^n = i_{Lj,ref}^{n-1}$. For the sake of simplicity, only average current-mode control has been employed to derive the discrete-time dynamics of the DC-link since it is the most recommendable type of control for PFC applications. It can be demonstrated that the reduced discrete-time dynamics of the DC-link voltage has the following expression.

$$v_C^{n+1} = v_C^n + \left(\frac{3i_{Lj,ref}^{n-1}}{C}\right)\left(\frac{L_j\left(i_{Lj,ref}^{n-1} - i_{Lj,ref}^n\right) + v_{in}^n T_{SW}}{v_C^n}\right) - \left(\frac{3v_{Bat}^n i_{Li,avg}^n}{Cv_C^n}\right)T_{SW} \tag{4.23}$$

Assuming that $i_{Lj,ref}^n = g^n \cdot v_{in}^n$ and $i_{Lj,ref}^{n-1} = g^{n-1} \cdot v_{in}^{n-1}$, that the computed conductance of the whole PFC stage (G^n) is three times the conductance of one boost cell (g^n), i.e. $G^n = 3g^n$, and that $3i_{Li,avg} = i_{Bat}^n$, equation (4.23) results in

$$v_C^{n+1} = v_C^n + \left(\frac{G^{n-1}v_{in}^{n-1}}{Cv_C^n}\right)\left(L_{eq}\left(G^{n-1}v_{in}^{n-1} - G^n v_{in}^n\right) + v_{in}^n T_{SW}\right) - \left(\frac{v_{Bat}^n i_{Bat}^n}{Cv_C^n}\right)T_{SW} \tag{4.24}$$

where L_{eq} stands for the equivalent value that results from the parallel connection of L_1, L_2 and L_3. Since $L_1 = L_2 = L_3$, L_{eq} is defined as $L_j/3$.

The previous recurrence describes the discrete-time dynamics of the DC-link voltage when the three inductor currents of the PFC stage are in sliding-mode regime.

Considering that around the equilibrium point $v_{in}^n = V_{in}$ (where V_{in} is the *RMS* value of the line voltage), $G^n = G^{n+1} = G$, $i_{Bat}^n = i_{Bat}^{n-1} = I_{Bat}$, $P_{in} = V_{in}^2 G$, $v_{Bat}^n = V_{Bat}$, and $P_{Bat} = V_{Bat} \cdot I_{Bat}$, the previous equation (4.24) results in

$$v_C^{n+1} = v_C^n + \left(\frac{T_{SW}}{Cv_C^n}\right)\left(P_{in} - P_{Bat}\right) \tag{4.25}$$

As it can be observed, v_C^{n+1} increases if the power absorbed from the grid is higher than the power absorbed from the DC-link capacitor and, in consequence, it decreases in the opposite situation. The DC-link voltage controller will ensure that a correct power balance is achieved so that the DC-link voltage is properly regulated.

4.2.3.3 Battery voltage ideal discrete-time dynamics

The reduced discrete-time dynamics of the battery voltage can be obtained if $i_{Li,avg}^n$ is substituted by $i_{Li,ref}^{n-1} = (i_{Bat,ref}^{n-1})/3$ in equation (3.42). As well as the previous case, only average current-mode control has been employed to derive the discrete-time dynamics of the battery voltage.

Hence, it can be demonstrated that the reduced discrete-time dynamics of the battery voltage is defined by the following expression.

$$v_{Bat}^{\,n+1} = v_{Bat}^{\,n}\left(1-\frac{T_{SW}}{R_o C_{Bat}}\right)+\left(\frac{i_{Bat,ref}^{\,n-1}}{C_{Bat}}\right)T_{SW} \tag{4.26}$$

The previous recurrence describes the discrete-time dynamics of the battery voltage when the three inductor currents of the BCR stage are in sliding-mode regime. Remember that R_o has been used to model the battery because experimental results will be performed with an electronic load in resistive configuration instead of a real battery (see Fig. 4.8).

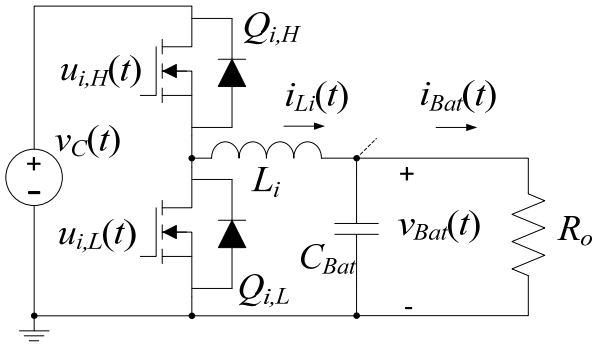


Fig. 4.5. Buck converter cell of the BCR stage cell with a resistive load that models the battery.

4.2.4 Equilibrium point

In this part, the equilibrium points of the whole system are derived. The corresponding equilibrium point of each boost converter is defined as $X_j^*=[I_{Lj},\ V_C]^T$ and the following assumptions have to be taken into account: $v_{in}^{\,n}=V_{in}$, $v_C^{\,n} = v_C^{\,n+1}=V_C$ and $G^n=G^{n+1}=G=3g$.

$$X_j^{\,*} = \begin{pmatrix} I_{Lj} \\ V_C \end{pmatrix} = \begin{pmatrix} gV_{in} \\ \dfrac{V_{in}^{\,2}G}{I_o} \end{pmatrix} \tag{4.27}$$

As it can be observed, inductor currents from the PFC stage are proportional to the input voltage and POPI conditions are demonstrated on the equilibrium point of the DC-link voltage. Therefore, it has been demonstrated that the PFC stage will behave as an LFR. However, it is important to remark that the DC-link voltage will not be constant because it is expected to exhibit a harmonic at twice the line frequency.

Similarly, the following assumptions are taken into account to derive the equilibrium point of buck converters $X_i^*=[I_{Li},\ V_{Bat}]^T$: $v_{Bat}^{\,n} = v_{Bat}^{\,n+1}= V_{Bat}$ and $i_{Li,ref}^{\,n-1}= i_{Bat,ref}^{\,n-1}/3= I_{Bat,ref}/3$. It can be demonstrated that the equilibrium point of the BCR stage is given by the following expression.

$$X_i^* = \begin{pmatrix} I_{Li} \\ V_{Bat} \end{pmatrix} = \begin{pmatrix} \frac{I_{Bat,ref}}{3} \\ I_{Bat,ref} R_o \end{pmatrix} \tag{4.28}$$

4.2.5 Stability analysis of the equilibrium point

4.2.5.1 Stability analysis in case of inductance mismatch

As commented previously, the proposed controller has to be considered as a predictive controller since it calculates the necessary control action τ_k^n at each switching period according to the sampled variables and the theoretical inductance value. However, the inductance value can vary depending on the load conditions, temperature, aging, etc. Hence, the stability of the system depends on the difference between the real inductance value ($L_{k,r}$) and the programmed value ($L_{k,p}$). Let us define m_r^n and m_p^n as the real and predicted slopes of inductor current for the n^{th} switching period respectively, where

$$m_r{}^n = \frac{v_{Lk}{}^n}{L_{k,r}} \tag{4.29}$$

$$m_p{}^n = \frac{v_{Lk}{}^n}{L_{k,p}} \tag{4.30}$$

and $v_{Lk}{}^n$ stands for voltage of inductor L_k during the n^{th} switching period, which is supposed to be correctly calculated.

On one hand, inductor current discrete-time dynamics is defined by (3.19) where slopes $m_1{}^n$ and $m_2{}^n$ stand for the real slopes of inductor current, so that (3.19) can be rewritten as follows.

$$i_{Lk}{}^{n+1} = i_{Lk}{}^n + \left(m_{1,r}{}^n - m_{2,r}{}^n\right)\tau_k{}^n + m_{2,r}{}^n T_{SW} \tag{4.31}$$

On the other hand, $m_1{}^n$ and $m_2{}^n$ of equivalent control $\tau_{eq,k}{}^n$ defined in (4.8) stand for the predicted slopes of the inductor current. In consequence, expression (4.8) can be rewritten as follows.

$$\tau_{eq,k}{}^n = \frac{\left(i_{Lk,ref}{}^n - i_{Lk}{}^n\right) - m_{2,p}{}^n T_{SW} - \left(m_{1,\mathrm{p}}{}^n \tau_{k,SS}{}^n\right) M}{m_{1,p}{}^n - m_{2,p}{}^n} \tag{4.32}$$

Considering that the control action τ_k^n is not saturated, it can be substituted in (4.31) for (4.32).

$$i_{Lk}{}^{n+1} = i_{Lk}{}^n + \left(m_{1,r}{}^n - m_{2,r}{}^n\right)\left(\frac{\left(i_{Lk,ref}{}^n - i_{Lk}{}^n\right) - m_{2,p}{}^n T_{SW} - \left(m_{1,\mathrm{p}}{}^n \tau_{k,SS}{}^n\right) M}{m_{1,p}{}^n - m_{2,p}{}^n}\right) + m_{2,r}{}^n T_{SW} \tag{4.33}$$

According to (4.29) and (4.30)

$$\frac{m_{1,r}{}^n - m_{2,r}{}^n}{m_{1,p}{}^n - m_{2,p}{}^n} = \frac{L_{k,p}}{L_{k,r}} \tag{4.34}$$

Hence, using (4.29), (4.30) and (4.34) in (4.33) yields to

$$i_{Lk}{}^{n+1} = i_{Lk}{}^{n}\left(1-\frac{L_{k,p}}{L_{k,r}}\right)+\frac{L_{k,p}}{L_{k,r}}i_{Lk,ref}{}^{n}-m_{1,r}{}^{n}\tau_{k,SS}{}^{n}M \tag{4.35}$$

Note that (4.35) is a recurrence, so that the order of the system is not actually reduced as in (4.15), in which $L_{k,r}= L_{k,p}$ was assumed. This means that in case of mismatch between the real and the programmed inductance value, inductor current will meet the reference after some switching periods if stability conditions are fulfilled. Next step is to study stability conditions of recurrence (4.35).

Let us define

$$\Delta i_{Lk}{}^{n+1} = i_{Lk}{}^{n+1} - i_{Lk}{}^{n} \tag{4.36}$$
$$\Delta i_{Lk}{}^{n} = i_{Lk}{}^{n} - i_{Lk}{}^{n-1} \tag{4.37}$$

where $i_{Lk}{}^{n}$ is defined as

$$i_{Lk}{}^{n} = i_{Lk}{}^{n-1}\left(1-\frac{L_{k,p}}{L_{k,r}}\right)+\frac{L_{k,p}}{L_{k,r}}i_{Lk,ref}{}^{n-1}-m_{1,r}{}^{n-1}\tau_{k,SS}{}^{n-1}M \tag{4.38}$$

Substituting (4.35) and (4.38) in (4.36) leads to

$$\begin{aligned}\Delta i_{Lk}{}^{n+1} &= i_{Lk}{}^{n}\left(1-\frac{L_{k,p}}{L_{k,r}}\right)+\frac{L_{k,p}}{L_{k,r}}i_{Lk,ref}{}^{n}-m_{1,r}{}^{n}\tau_{k,SS}{}^{n}M-i_{Lk}{}^{n-1}\left(1-\frac{L_{k,p}}{L_{k,r}}\right)+\\ &+\frac{L_{k,p}}{L_{k,r}}i_{Lk,ref}{}^{n-1}-m_{1,r}{}^{n-1}\tau_{k,SS}{}^{n-1}M\end{aligned} \tag{4.39}$$

Assuming that $i_{Lk,ref}{}^{n}= i_{Lk,ref}{}^{n-1}$, $m_{1,r}{}^{n}= m_{1,r}{}^{n-1}$ and $\tau_{k,SS}{}^{n}= \tau_{k,SS}{}^{n-1}$ makes possible rewriting (4.39) as

$$\Delta i_{Lk}{}^{n+1} = \Delta i_{Lk}{}^{n}\left(1-\frac{L_{k,p}}{L_{k,r}}\right) \tag{4.40}$$

The previous recurrence will be stable as long as

$$0 < L_{k,p} < 2L_{k,r} \tag{4.41}$$

This implies that the system will be stable if the programmed inductance value is positive and lower than twice the real inductance. It is worth commenting that these stability conditions are in concordance to the ones reported in [102].

The decrease of inductance value is mostly generated by the increase of load conditions. In the particular case of the employed inductors, they exhibit a maximum inductance deviation of 40% between the minimum and the maximum load conditions. For that reason, the programmed value should correspond to the inductance exhibited under maximum load conditions, this ensuring the stability conditions for the whole operation range.

Moreover, the inductance mismatch produces another effect in steady state conditions. This effect consists in an undesired offset of i_{Lk}^{n} samples with respect the expected ones. In steady state $i_{Lk}^{n+1}=i_{Lk}^{n}$, $i_{Lk,ref}^{n}=i_{Lk,ref}^{n-1}$ and $m_{1,r}^{n}=m_{1,r}^{n-1}$ so that (4.35) becomes

$$i_{Lk}^{n} = i_{Lk,ref}^{n} - \frac{L_{k,r}}{L_{k,p}} m_{1,r}^{n} \tau_{k,SS}^{n} M \tag{4.42}$$

instead of (4.15) which has the following form

$$i_{Lk}^{n} = i_{Lk,ref}^{n} - m_{1,r}^{n} \tau_{k,SS}^{n} M \tag{4.43}$$

Hence, the undesired offset can be defined by the following expression

$$\Delta i_{Lk,offset}^{n} = m_{1,r}^{n} \tau_{k,SS}^{n} M \left(\frac{L_{k,r}}{L_{k,p}} - 1 \right) \tag{4.44}$$

However, this effect is expected to be compensated by the action of the outer loops.

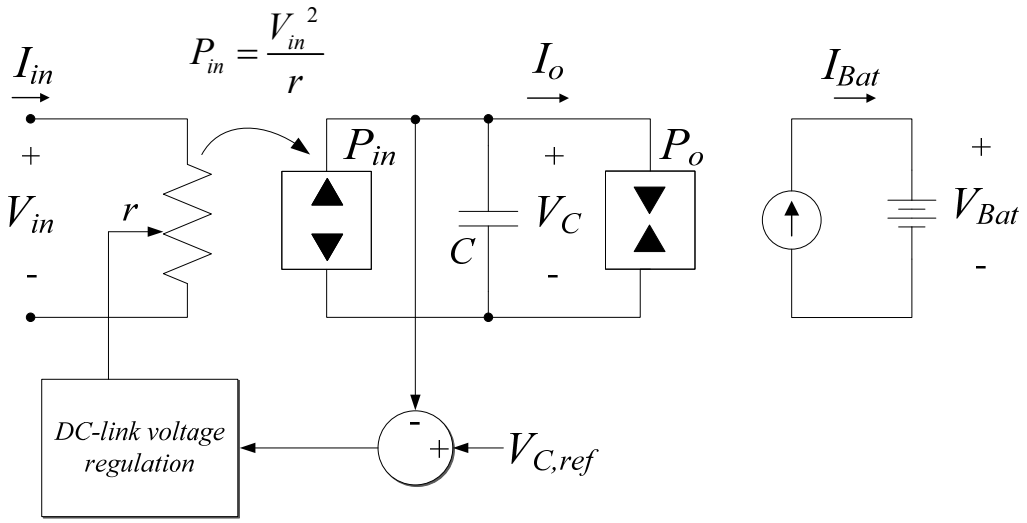


Fig. 4.6. Large-signal averaged system's modelling.

4.2.5.2 Stability of the DC-link voltage equilibrium point

Stability of the DC-link voltage capacitor has to be ensured by the DC-link voltage controller. As it can be observed in Fig. 4.6 the DC-link capacitor is charged by the PFC, which is behaving as an LFR, and discharged by the second stage, which behaves as a constant power load with respect the DC-link capacitor. Therefore, the DC-link voltage will remain at the desired level of voltage as long as the DC-link voltage controller ensures a properly balanced power conditions between the absorbed power from the grid and the power delivered to the battery.

4.2.5.3 Stability of the battery voltage equilibrium point

Considering that $i_{Bat,ref}^{n}=i_{Bat,ref}^{n-1}=I_{Bat,ref}$, equation (4.26) results in

$$v_{Bat}^{n+1} = v_{Bat}^{n}\left(1-\frac{T_{SW}}{R_o C_{Bat}}\right)+\left(\frac{I_{Bat,ref}}{C_{Bat}}\right)T_{SW} \tag{4.45}$$

By defining

$$\Delta v_{Bat}^{n} = v_{Bat}^{n} - v_{Bat}^{n-1} \tag{4.46}$$

$$\Delta v_{Bat}^{n+1} = v_{Bat}^{n+1} - v_{Bat}^{n} \tag{4.47}$$

Equation (4.47) can be rewritten as

$$\begin{aligned}\Delta v_{Bat}^{n+1} &= \left(v_{Bat}^{n}\left(1-\frac{T_{SW}}{R_o C_{Bat}}\right)+\left(\frac{I_{Bat,ref}}{C_{Bat}}\right)T_{SW}\right)-\left(v_{Bat}^{n-1}\left(1-\frac{T_{SW}}{R_o C_{Bat}}\right)+\left(\frac{I_{Bat,ref}}{C_{Bat}}\right)T_{SW}\right)= \\ &= \Delta v_{Bat}^{n}\left(1-\frac{T_{SW}}{R_o C_{Bat}}\right)\end{aligned} \tag{4.48}$$

Hence, equation (4.48) will be stable as long as

$$\left|1-\frac{T_{SW}}{R_o C_{Bat}}\right|<1 \tag{4.49}$$

which is always satisfied since $T_{SW}<<R_oC_{Bat}$ even for the lowest value of R_o.

4.3 Design of the DC-link voltage regulation loop

As commented previously, the DC-link voltage controller has been added to ensure that the DC-link voltage remains at the desired voltage level. As it can be observed in Fig. 4.7, this control loop computes the corresponding conductance reference G^n that defines inductor current reference $i_{Lj,ref}^{n}$ for the PFC inductor current controllers.

Before designing this control loop in the z-plane, the conductance reference to DC-link voltage transfer function ($G_{GVc}(z)$) has to be calculated from the reduced-order non-linear dynamics of the DC-link voltage which is defined in (4.24). If (4.24) is linearized by means of a first order Taylor's approximation around the equilibrium point, it results in the following small-signal discrete-time recurrence of the DC-link voltage.

$$\begin{aligned}\tilde{v}_C^{\,n+1} \simeq &\left.\frac{\partial v_C^{\,n+1}}{\partial v_C^{\,n}}\right|_{X^*}\tilde{v}_C^{\,n}+\left.\frac{\partial v_C^{\,n+1}}{\partial G^{n}}\right|_{X^*}\tilde{G}^{n}+\left.\frac{\partial v_C^{\,n+1}}{\partial G^{n-1}}\right|_{X^*}\tilde{G}^{n-1}+\left.\frac{\partial v_C^{\,n+1}}{\partial v_{in}^{\,n}}\right|_{X^*}\tilde{v}_{in}^{\,n}+\left.\frac{\partial v_C^{\,n+1}}{\partial v_{in}^{\,n-1}}\right|_{X^*}\tilde{v}_{in}^{\,n-1}+ \\ &+\left.\frac{\partial v_C^{\,n+1}}{\partial v_{Bat}^{\,n}}\right|_{X^*}\tilde{v}_{Bat}^{\,n}+\left.\frac{\partial v_C^{\,n+1}}{\partial i_{Bat}^{\,n}}\right|_{X^*}\tilde{i}_{Bat}^{\,n}\end{aligned} \tag{4.50}$$

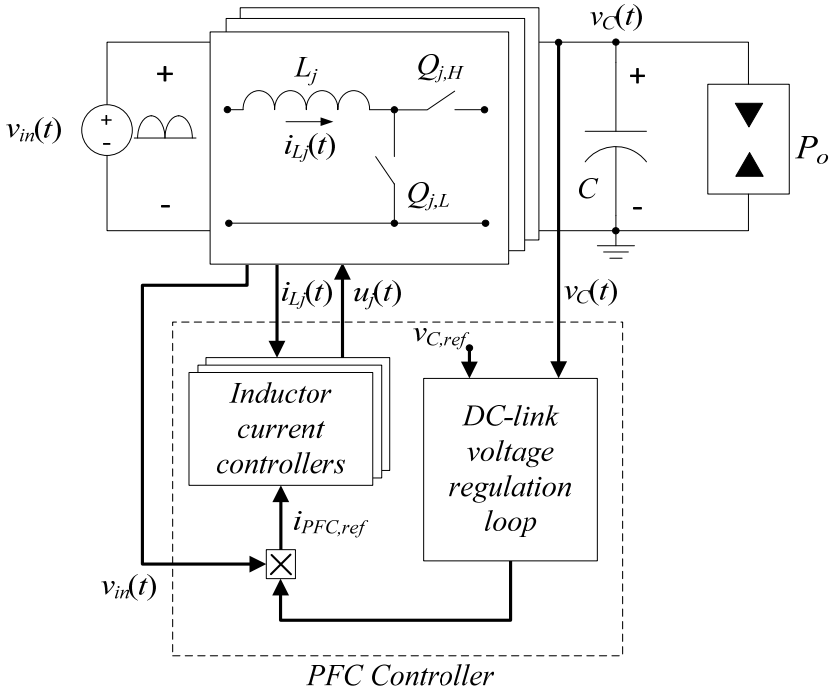


Fig. 4.7. PFC controller stage of the battery charger.

where

$$\left.\frac{\partial v_C^{\,n+1}}{\partial v_C^{\,n}}\right|_{X^*} = 1+\frac{T_{SW}}{CV_C^{\,2}}\left(I_{Bat}V_{Bat}-GV_{in}^{\,2}\right) \tag{4.51}$$

$$\left.\frac{\partial v_C^{\,n+1}}{\partial G^{n}}\right|_{X^*} = -\frac{L_{eq}GV_{in}^{\,2}}{CV_C} \tag{4.52}$$

$$\left.\frac{\partial v_C^{\,n+1}}{\partial G^{n-1}}\right|_{X^*} = \frac{V_{in}^{\,2}}{CV_C}\left(L_{eq}G+T_{SW}\right) \tag{4.53}$$

$$\left.\frac{\partial v_C^{\,n+1}}{\partial v_{in}^{\,n}}\right|_{X^*} = \frac{GV_{in}}{CV_C}\left(-L_{eq}G+T_{SW}\right) \tag{4.54}$$

$$\left.\frac{\partial v_C^{\,n+1}}{\partial v_{in}^{\,n-1}}\right|_{X^*} = \frac{GV_{in}}{CV_C}\left(L_{eq}G+T_{SW}\right) \tag{4.55}$$

$$\left.\frac{\partial v_C^{\,n+1}}{\partial i_{Bat}^{\,n}}\right|_{X^*} = -\frac{T_{SW}V_{Bat}}{CV_C} \tag{4.56}$$

$$\left.\frac{\partial v_C^{\,n+1}}{\partial v_{Bat}^{\,n}}\right|_{X^*} = -\frac{T_{SW}I_{Bat}}{CV_C} \tag{4.57}$$

Besides, $I_{Bat}V_{Bat}=GV_{in}^{\,2}$ if the system is in steady state implies that, then (4.51) becomes

$$\left.\frac{\partial v_C^{\,n+1}}{\partial v_C^{\,n}}\right|_{X^*} = 1 \tag{4.58}$$

Meaning that $v_C^{\,n+1}=v_C^{\,n}$.

The DC-link voltage small-signal dynamics can be modelled as in Fig. 4.8, in which the contribution of each perturbation signal to the DC-link voltage signal depends on a different discrete-time transfer function. Perturbation signals are the conductance reference, the rectified input voltage, the battery voltage and the battery current. The respective transfer functions are obtained by neglecting the rest of perturbation signals and applying a *z*-transformation on recurrence (4.50). These transfer functions are summarised in Table 4.3.

Note that $G_{GVc}(z)$ exhibits two poles, one in the centre of the unity circle and one pure integrator. It also has a non-minimum phase high-frequency zero outside of the unity circle. DC-link voltage controllers are generally designed with a cut-off frequency below the 20 Hz to avoid distorting the current absorbed from the grid [105]. Therefore, it is possible to simplify $G_{GVc}(z)$ by considering that z=1 in the numerator because the contribution of the high-frequency zero can be neglected for low-frequency conditions. In consequence, $G_{GVc}(z)$ results in

$$G_{GVc}(z) = \left(\frac{V_{in}{}^2 T_{SW}}{C V_C} \right) \frac{1}{z(z-1)} \tag{4.59}$$

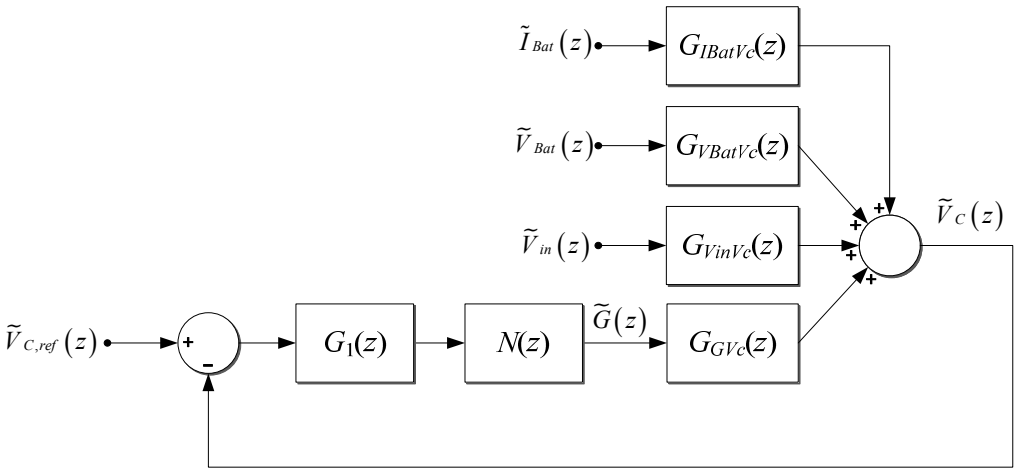


Fig. 4.8. Small-signal model of the DC-link voltage with sliding-mode current control and outer voltage control loop.

As it can be seen in Fig. 4.8, the DC-link voltage regulation loop is composed by transfer functions $G_1(z)$, $N(z)$ and $G_{GVc}(z)$. $G_1(z)$ stands for the discrete-time PI voltage controller that carries out the DC-link voltage regulation while $N(z)$ is a Notch filter that attenuates the $G_1(z)$ output component at twice the line frequency. It is important to remark that the use of a Notch filter is optional but it is very suitable to achieve a higher power factor because it can highly reduce the third harmonic amplitude of current $i_{AC}(t)$.

Transfer function	Symbol	Expression
Conductance reference to DC-link voltage	$G_{GVc}(z)$	$G_{GVc}(z) = -\left(\frac{GV_{in}{}^2 L_{eq}}{CV_C}\right)\frac{\left(z-\left(1+\frac{T_{SW}}{GL_{eq}}\right)\right)}{z(z-1)}$
Input voltage to DC-link voltage	$G_{VinVc}(z)$	$G_{VinVc}(z) = -\left(\frac{GV_{in}\left(L_{eq}G-T_{SW}\right)}{CV_C}\right)\frac{\left(z-\frac{\left(L_{eq}G+T_{SW}\right)}{\left(L_{eq}G-T_{SW}\right)}\right)}{z(z-1)}$
Battery voltage to DC-link voltage	$G_{VBatVc}(z)$	$G_{VBatVc}(z) = -\left(\frac{T_{SW}V_{Bat}}{CV_C}\right)\frac{1}{(z-1)}$
Battery current to DC-link voltage	$G_{IBatVc}(z)$	$G_{IBatVc}(z) = -\left(\frac{T_{SW}I_{Bat}}{CV_C}\right)\frac{1}{(z-1)}$

Table 4.3. Small-signal perturbation signals to DC-link voltage transfer functions.

Besides, it is worth noting that it is not necessary to execute the DC-link voltage controller algorithm every switching period because $v_C(t)$ is not expected to vary so much within this time owing to the relatively high DC-link capacitance. Moreover, if the DC-link voltage controller was designed to be calculated every switching period, it would result in a very low proportional gain in order to achieve the required low cut-off frequency, which can eventually lead to computation errors in case that the digital controller does not have enough decimal resolution. In contrast, designing a DC-link voltage controller to be executed less frequently results in a more efficient controller in terms of necessary computational resources and a higher proportional gain for the same cut-off frequency, which can avoid possible computation derived errors.

For that reason, the DC-link voltage controller has been designed to be executed every 6 switching periods T_{SW} of a single cell. This implies that if the switching frequency of the system is 60 kHz, the DC-link voltage controller will be executed at a frequency rate of 10 kHz. Hence, the execution period of the DC-link voltage regulation loop algorithm T_{S2} comes defined as

$$T_{S2} = 6T_{SW} \tag{4.60}$$

Hence, to design the DC-link voltage controller properly, T_{SW} in equation (4.59) has to be substituted for T_{S2}. It must be commented that this frequency rate reduction has been selected experimentally. It has been seen that a higher rate decrease introduces a noticeable distortion

into the line current. In addition, this frequency-rate reduction might eventually lead to instability issues for lower DC-link capacitance conditions.

The *z*-plane transfer function of the proposed discrete-time PI voltage controller has the following form.

$$G_1(z) = k_p \frac{(z - z_0)}{(z - 1)} \tag{4.61}$$

As it can be observed, $G_1(z)$ exhibits one integrator, one real zero at z_0 and a proportional gain k_p. Zero z_0 has to be set to give sufficient phase-margin to the system while k_p has to be adjusted according to the desired cut-off frequency.

As commented previously, a Notch filter $N(z)$ has been included in the DC-link voltage regulation loop in order to mitigate the effect that the DC-link voltage ripple has on the line current. As it will be seen later on, the use of a Notch filter results in a higher PF and lower total harmonic distortion (THD) due to the high attenuation of the third harmonic of line current $i_{AC}(t)$.

The general expression of the Notch filter here employed is given by the following expression

$$N(z) = \frac{z^2 + b_1 z + 1}{z^2 + a_1 z + a_2} \tag{4.62}$$

where

$$b_1 = -2\cos(\omega_N) \tag{4.63}$$
$$a_1 = -2r\cos(\omega_N) \tag{4.64}$$
$$a_2 = r^2 \tag{4.65}$$

Parameter r stands for the quality factor of the filter and ω_N is defined as the discrete centre frequency, which is defined by the following expression

$$\omega_N = 2\pi \frac{f_N}{f_{S2}} \tag{4.66}$$

where f_N is the frequency that the filter has to attenuate, i.e. 100 Hz if the line frequency is 50 Hz, and f_{S2} is the inverse of T_{S2}.

The PI controller has been designed taking into account parameters of Table 4.4 in order to adjust of the cut-off frequency of the system at 20 Hz, which is considered sufficiently below the rectified input voltage frequency to avoid distorting the line current. The quality factor r of the Notch filter has been adjusted at 0.99 and f_N at 100 Hz because experimental results will be carried out for a line frequency of 50 Hz. For a line frequency of 60 Hz, f_N should be 120 Hz.

Parameter	Value
V_{in}	230 V_{RMS}
V_C	400 V
T_{S2}	100 μs
C	1200 μF

Table 4.4. Design parameters for the DC-link voltage controller.

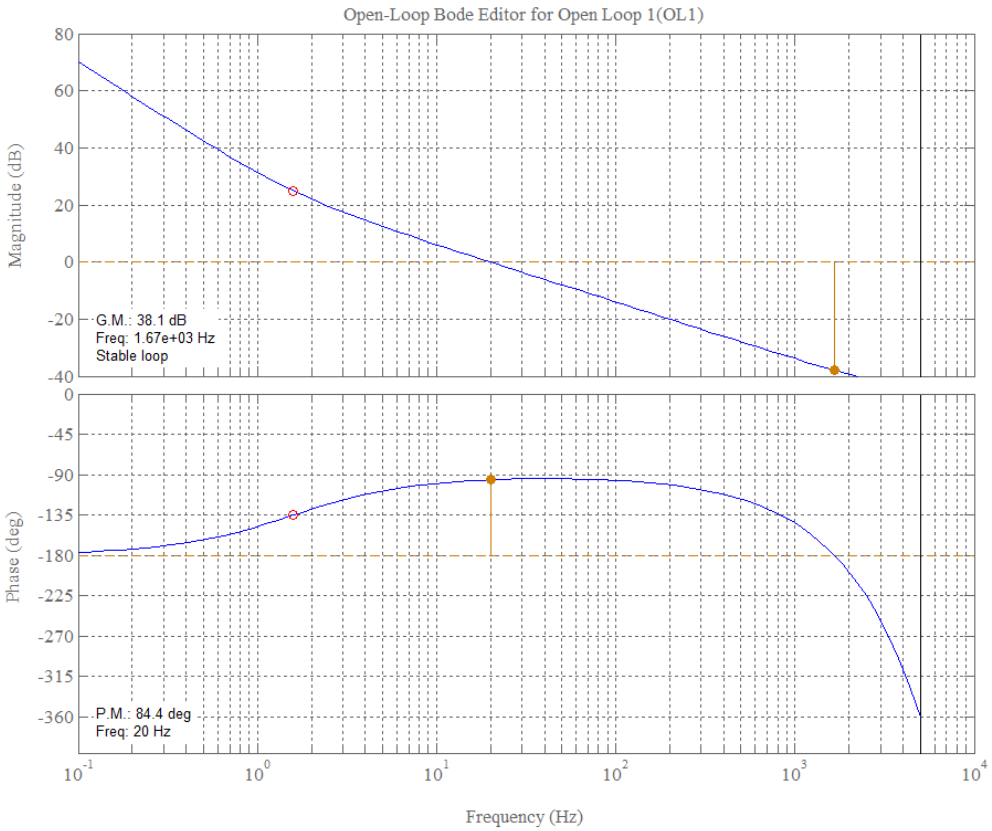
The different parameters of the DC-link voltage regulation loop are summarised in Table 4.5. Fig. 4.9.a depicts the Bode diagram of the system's loop gain without the Notch filter, while Fig. 4.9.b illustrates the Bode diagram when the loop includes the Notch filter. As it can be observed, the main difference between both Bode diagrams is the high attenuation of the system's loop gain magnitude at 100 Hz that is visible in Fig. 4.9.b due to the Notch filter application. Note also that the presence of the Notch filter only reduces the cut-off frequency from 20 Hz to 19.6 Hz and the phase-margin from 84.4º to 80.7º.

Configuration of the DC-link voltage regulation	Constant parameter	Values
PI controller	z_o	0.999
	k_p	$1.135 \cdot 10^{-3}$
Notch filter	a_1	-1.9761
	a_2	0.9801
	b_1	-1.9961
	r	0.99
	ω_N	$62.8 \cdot 10^{-3}$

Table 4.5. Parameter values of the DC-link voltage regulation loop.

The implementation of $G_1(z)$ and $N(z)$ is illustrated by the block diagrams depicted in Fig. 4.10.a and Fig. 4.10.b respectively. As it can be observed, $G_1(z)$ generates a temporal value of conductance reference (G_o^m) periodically every T_{S2}. The calculated conductance is filtered by the Notch filter $N(z)$ or directly assigned to the conductance reference G^n depending on if the Notch filter is used or not.

a)



b)

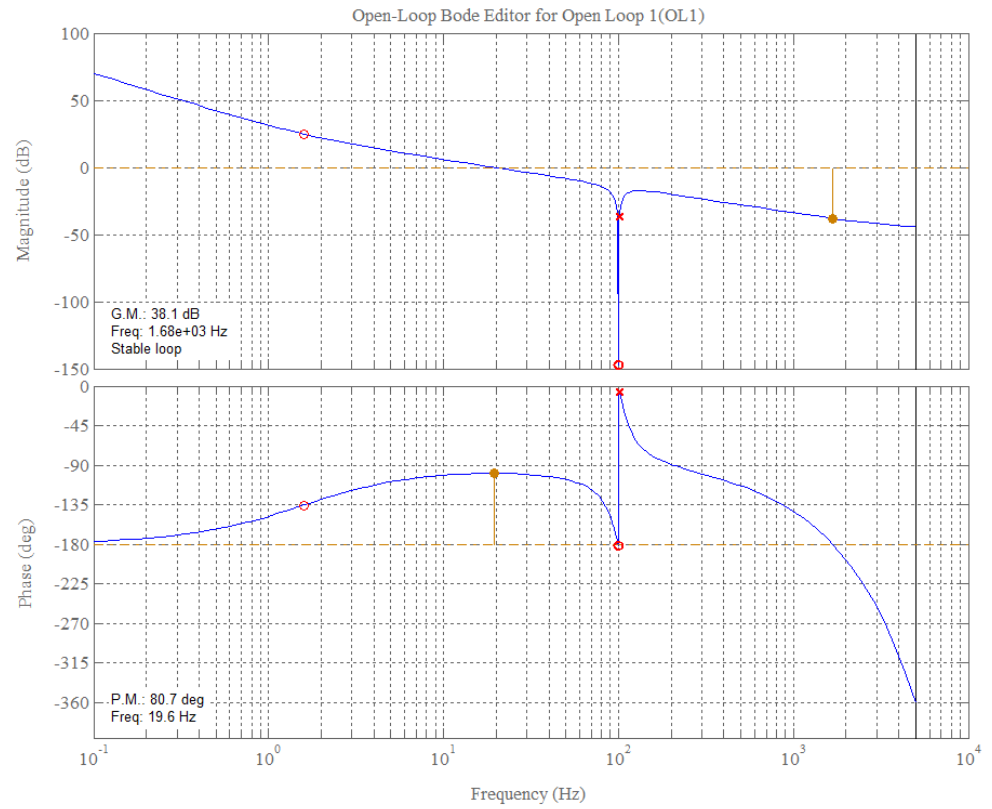


Fig. 4.9. Bode diagram of the DC-link voltage regulation gain loop. PI voltage controller a) without Notch filter, b) with Notch filter.

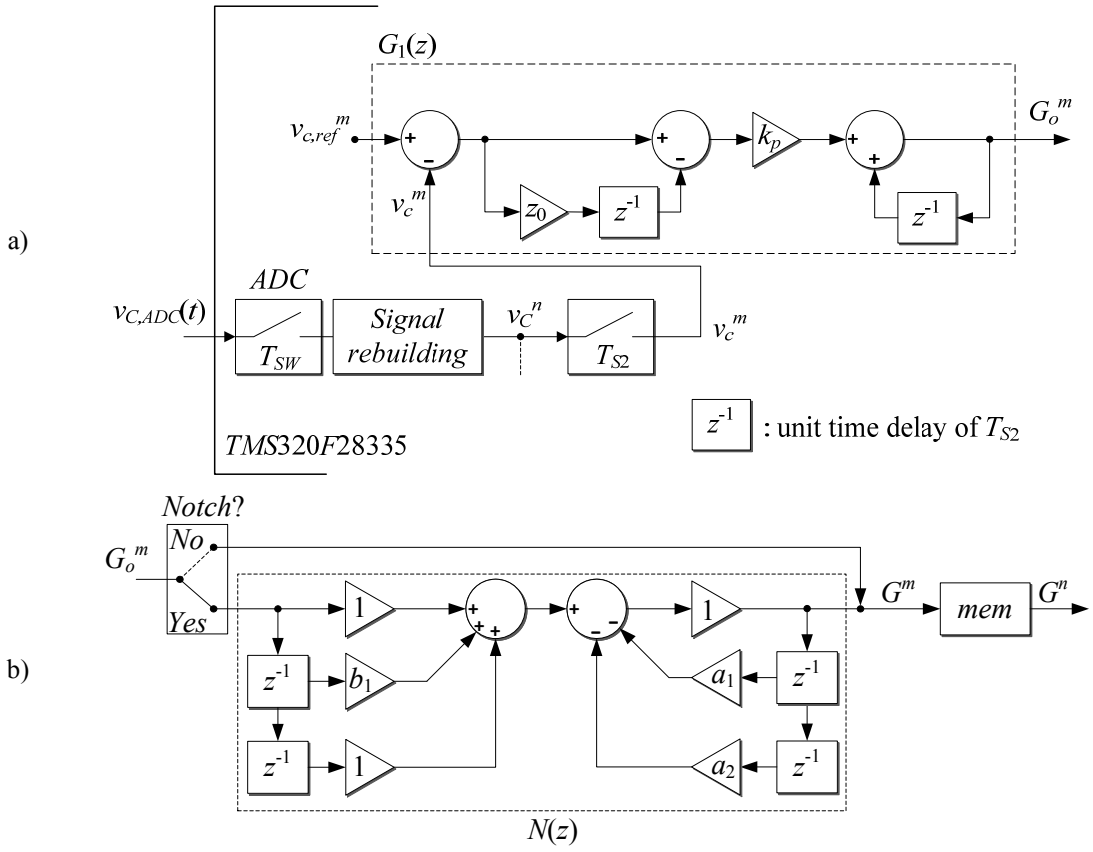


Fig. 4.10. Block diagram implementation of a) $G_1(z)$, b) $N(z)$

4.4 Battery voltage controller design

A similar procedure to the DC-link voltage regulation loop is followed to design the battery voltage outer control loop. In this case, the outer controller computes the battery current reference that defines the inductor current reference $i_{Li,ref}^{\ n}$ for the current-mode controllers of the second stage.

Firstly, the battery current reference to battery voltage transfer function ($G_{IBat,ref\text{-}VBat}(z)$) is calculated from the reduced-order discrete-time dynamics of the battery voltage defined in (4.26). Linearizing is not necessary in this case since (4.26) is already linear. Thus, it can be directly transformed into z-plane as follows.

$$G_{IBat,ref-VBat}(z)=\frac{\tilde{V}_{Bat}(z)}{\tilde{I}_{Bat,ref}(z)}=\left(\frac{T_{SW}}{C_{Bat}}\right)\frac{1}{z\left(z-\left(1-\frac{T_{SW}}{R_oC_{Bat}}\right)\right)} \tag{4.67}$$

Similarly to the DC-link voltage controller, the z-plane transfer function of the proposed PI battery voltage controller has the following form

$$G_2(z)=k_{p,Bat}\frac{(z-z_{0,Bat})}{(z-1)} \tag{4.68}$$

In this case, if $k_{p,Bat}$ and $z_{0,Bat}$ are adjusted to 0.1295 and 0.9926 respectively taking into account the parameters listed in Table 4.6, the system exhibits the cut-off frequency at approximately 700 Hz with a phase-margin of 60º (see Fig. 4.11).

Parameter	Value
P_{Bat}	3 kW
V_{Bat}	380 V
$R_o=(V_{Bat})^2/P_{Bat}$	48.13 Ω
C_{Bat}	30 µF

Table 4.6. Design parameters for the battery voltage controller.

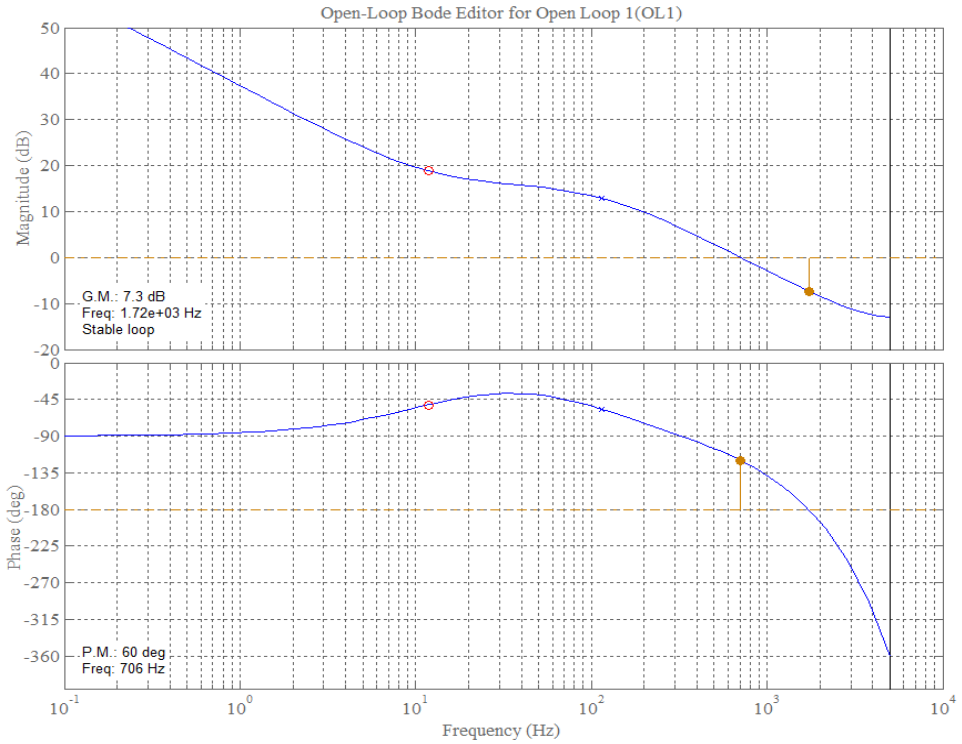


Fig. 4.11. Magnitude and phase of the battery voltage regulation gain loop.

4.5 Sequential execution of the control algorithm

Probably the reader has noticed that the interleaving operation of the different cells has not been considered to model the power converters in the previous chapter. This is because the interleaving operation does not have any special influence on the definition of the derived discrete-time models. However, it does have an important impact on the sequential operation of the control algorithm.

The interleaved operation of PFC cells is depicted in Fig. 4.12. The control sequence starts at t_a^n for normal operation conditions, continues at $t_b^n = t_a^n + T_{SW}/3$, at $t_c^n = t_b^n + T_{SW}/3$ and finishes at t_a^{n+1}. In addition, it is important to remark that control signal $u_1(t)$ is in phase with $u_4(t)$, in

consequence, $u_2(t)$ is in phase with $u_5(t)$ and $u_3(t)$ with $u_6(t)$. The complete sequential execution is detailed below and illustrated in Fig. 4.13.

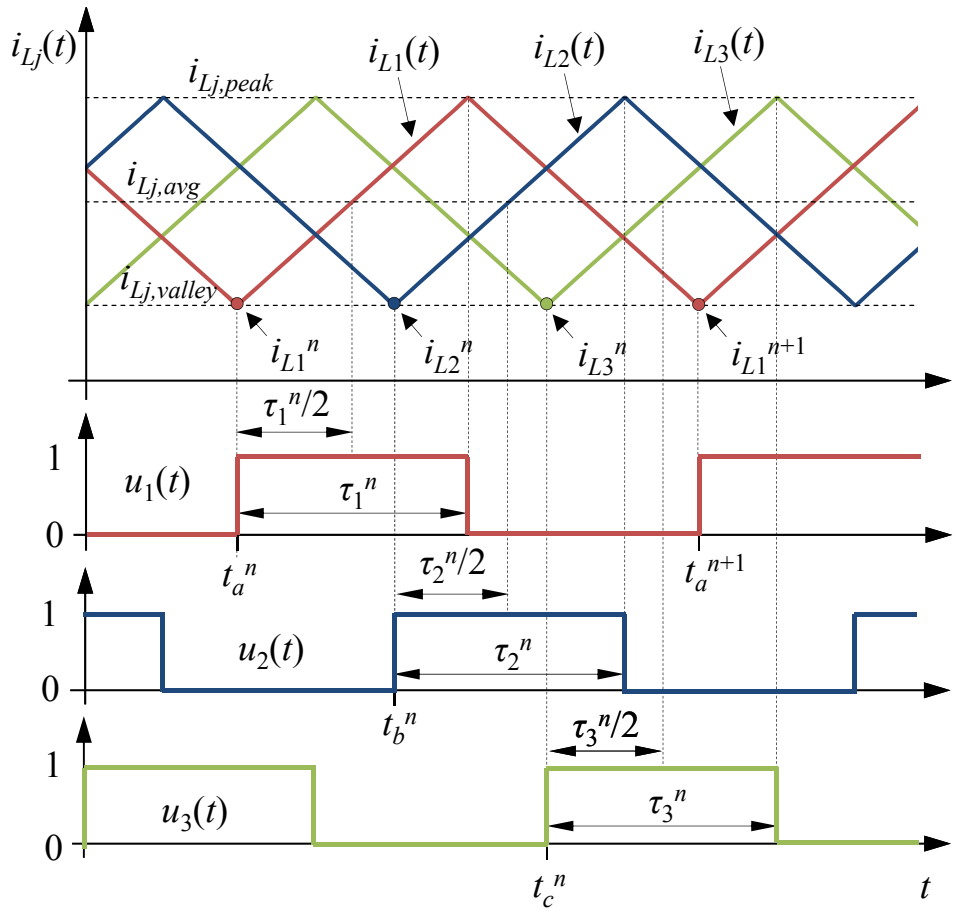


Fig. 4.12. Interleaving operation example. Interleaved inductor currents $i_{Lj}(t)$ and control signals $u_j(t)$.

Control sequence:

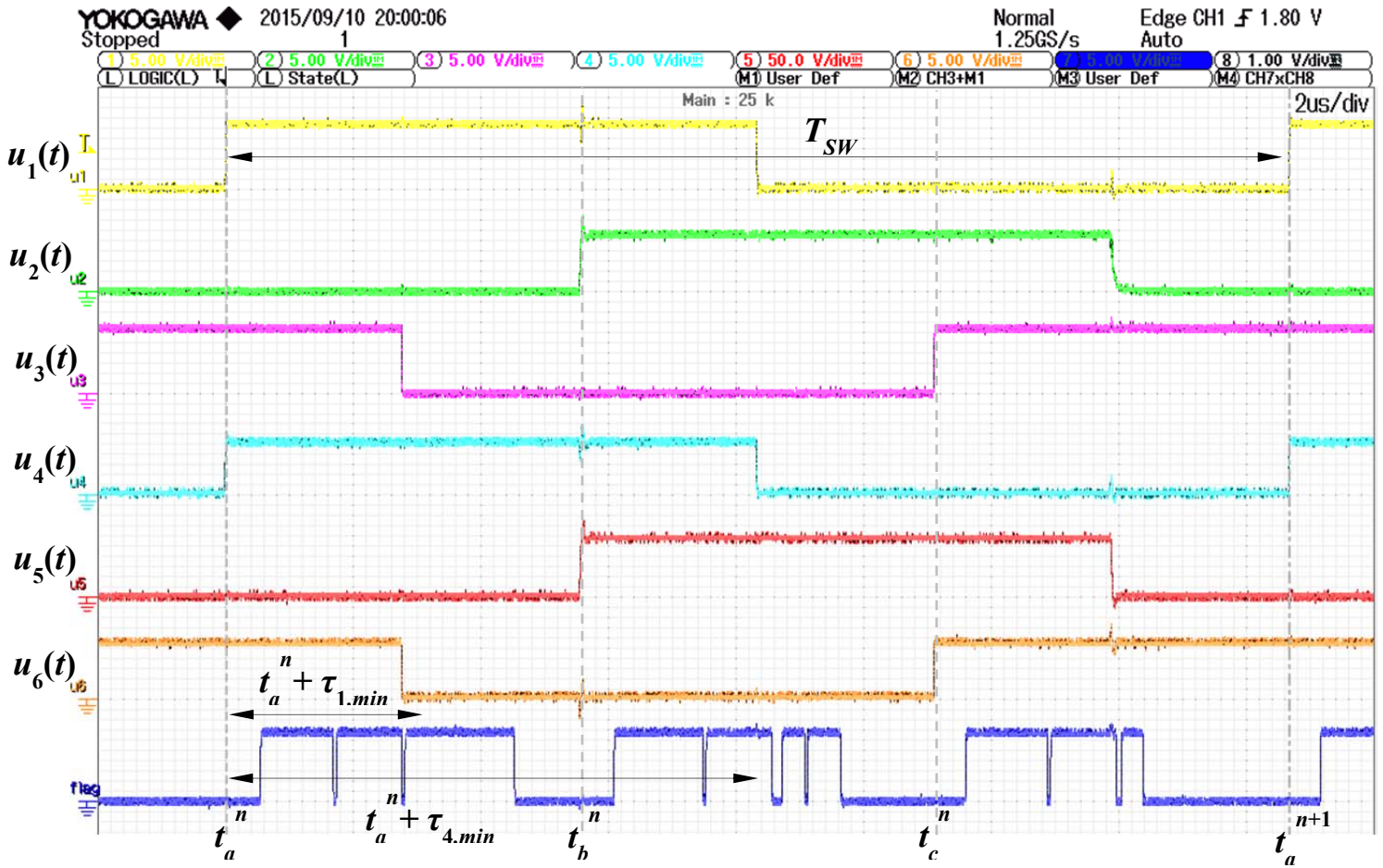
1. Signals $i_{L1,ADC}(t)$, $i_{L4,ADC}(t)$ and $v_{C,ADC}(t)$ are sampled sequentially just before that control signals $u_1(t)$ and $u_4(t)$ switch ON ($t=t_a^n$).
2. Sample i_{L1}^n is rebuilded, current control $d_1^n(\tau_1^n)$ is computed and the resulting duty cycle is sent to the DPWM module that generates $u_1(t)$.
3. Sample i_{L4}^n is rebuilded, current control $d_4^n(\tau_4^n)$ is computed and the resulting duty cycle is sent to the DPWM module that generates $u_4(t)$.
4. Sample v_C^n is rebuilded and division $1/v_C^n$ is calculated to be used in all inductor current controllers.
5. Wait until t_b^n.
6. Signals $i_{L2,ADC}(t)$, $i_{L5,ADC}(t)$ and $v_{in,ADC}(t)$ are sampled sequentially just before that control signals $u_3(t)$ and $u_6(t)$ switch ON ($t=t_b^n$).

7. Samples i_{L2}^{n} and v_{in}^{n} are rebuilded, PFC inductor current reference $i_{Lj,ref}^{n}$ is calculated as $g^n \cdot v_{in}^{n}$, current control $d_2^n(\tau_2^n)$ is computed and the result is sent to the DPWM module that generates $u_2(t)$.
8. Sample i_{L5}^{n} is rebuilded, current control $d_5^n(\tau_5^n)$ is computed and the result is sent to the DPWM module that generates $u_5(t)$.
9. If this is the 6^{th} sequence after the last execution of voltage controller $G_1(z)$ and Notch filter $N(z)$, then execute:
   a. $G_1(z)$ and
   b. $N(z)$ to update conductance g^n.
10. Wait until t_c^{n}.
11. Signals $i_{L3,ADC}(t)$, $i_{L6,ADC}(t)$ and $v_{Bat,ADC}(t)$ are sampled sequentially just before that control signals $u_3(t)$ and $u_6(t)$ switch ON ($t=t_c^{n}$).
12. Sample i_{L3}^{n} is rebuilded, current control $d_3^n(\tau_3^n)$ is computed and the result is sent to the DPWM module that generates $u_3(t)$.
13. Samples i_{L6}^{n} and v_{Bat}^{n} are rebuilded, current control $d_6^n(\tau_6^n)$ is computed and the result is sent to the DPWM module that generates $u_6(t)$.
14. If this is the 6^{th} sequence after the last execution of battery voltage controller $G_2(z)$, then calculate $G_2(z)$ to update $i_{Li,ref}^{n}$.
15. Wait until t_a^{n+1}.

Signal $ct(t)$ in Fig. 4.13 represents the computation time of each part of the previous sequence. Numbers at the bottom of the figure correspond to each numbered part of the sequence, so that it is possible to measure how long the computation of each part is. As it can be observed, the longest computation part corresponds to the division operation (point 4). Moreover, Fig. 4.13 demonstrates that the calculated duty cycle can be applied on the same switching period since the computation time of inductor current-mode controllers is lower than the minimum duty cycles reported in Table 4.7. Finally, it is worth commenting that duty cycle of all $u_k(t)$ signals have been adjusted at 0.5 only for illustration purposes.

Stage	**General duty cycle expression**	**Conditions**	$d_{min}(t)$	$\tau_{k,min}$
PFC	$d(t) = 1 - \frac{v_{in}(t)}{v_C(t)}$	$v_{in}(t)$=325.27 V; $v_C(t)$=390 V	0.1660	2.77 µs
BCR	$d(t) = \frac{v_{Bat}(t)}{v_C(t)}$	$v_{Bat}(t)$=200 V; $v_C(t)$=410 V	0.4878	8.13 µs

Table 4.7. Minimum duty cycles in each stage under steady-state operation conditions.



1	2	3	4	5	6	7	8	9.a	9.b	10	11	12	13	14	15

ct(t) (computation time)

Fig. 4.13. Execution sequence.

4.6 Conclusions

The design of the digital controllers has been presented in this chapter. Inductor current-mode controllers have been obtained from the application of the discrete-time SMC theory while voltage regulators have been designed by means of discrete-time PI controllers. The average-mode control technique has been selected for all inductor current-mode controllers, mainly to achieve a high PFC from the PFC stage. As demonstrated, the digital control design of the different state variables requires the use of their discrete-time modelling equations, which were previously obtained in Chapter 3.

An LFR behaviour has been imposed on the first stage by means of the proposed control strategy, whose emulated input resistive (or conductance) characteristic is regulated by the DC-link voltage controller to maintain the DC-link voltage at the desired voltage level. A Notch filter has been added in the DC-link voltage regulation loop to remove the low-frequency oscillations at twice the line frequency from the computed conductance. This results in an important attenuation of the third harmonic of the line current. On the other hand, the BCR controller imposes the CC or CV operation depending on the battery voltage.

Finally, the feasibility of the proposed control execution sequence in a single TMS320F28335 DSC from TEXAS INSTRUMENTS to manage the whole battery charger has been demonstrated by illustrating the required computation-time of each part of the control algorithm.

UNIVERSITAT ROVIRA I VIRGILI
DESIGN AND CONTROL OF A BATTERY CHARGER FOR ELECTRIC VEHICLES
Adrià Marcos Pastor

Chapter 5

SIMULATION AND EXPERIMENTAL RESULTS

This chapter aims to demonstrate the feasibility of the designed digital controllers on the designed battery charger through different simulation and experimental results. Simulation results have been carried out by means of the PSIM package while the experimental results have been obtained from the implemented battery charger prototype.

5.1 PSIM simulation model

Fig. 5.1 depicts the PSIM model of the battery charger power stage. In particular, Fig. 5.1.a illustrates the synchronised rectifier and the three boost converters connected in parallel that configure the first stage of the battery charger. As it can be observed, signals $v_{in}(t)$, $v_C(t)$ and the three inductor currents are sensed to be sent to the digital controller. On the other hand, Fig. 5.1.b depicts the second stage, which is based on three buck converters connected in parallel, and a voltage controlled current source that emulates the battery. As it can be observed, the load current is given by the division between the battery voltage and the load resistance so that the SoC of the battery can be emulated externally by parameter R_o. In this case, the three inductor currents of the second stage and the battery voltage are sensed to compute the control algorithm.

In Fig. 5.2 it is possible to see how the sensed battery charger signals are sampled with different sample and hold blocks to emulate the data acquisition from the DSC through its ADCs. Two groups of three square signals have been used to synchronise the operation of the control algorithm. Three square signals with a frequency of f_{SW}=60 kHz and a phase-shift of 120º between them are employed to synchronise the moment the different samples are taken. As it can be seen, it corresponds with the sequence operation that has been explained previously in section 4.5. Sample & hold blocks get the information when the triggering signal changes from low to high, i.e., at the beginning of their period. The other three square signals used for synchronisation purposes have also a phase-shift of 120º between them but a frequency of f_2=10 kHz. These slower signals are used for triggering the algorithm of the DC-link voltage controller, the notch filter and the battery voltage controller. Three saw-tooth signals with a

frequency of 60 kHz and 120º of phase-shift have been used to generate PWM control signals that are generated by the inductor current controllers.

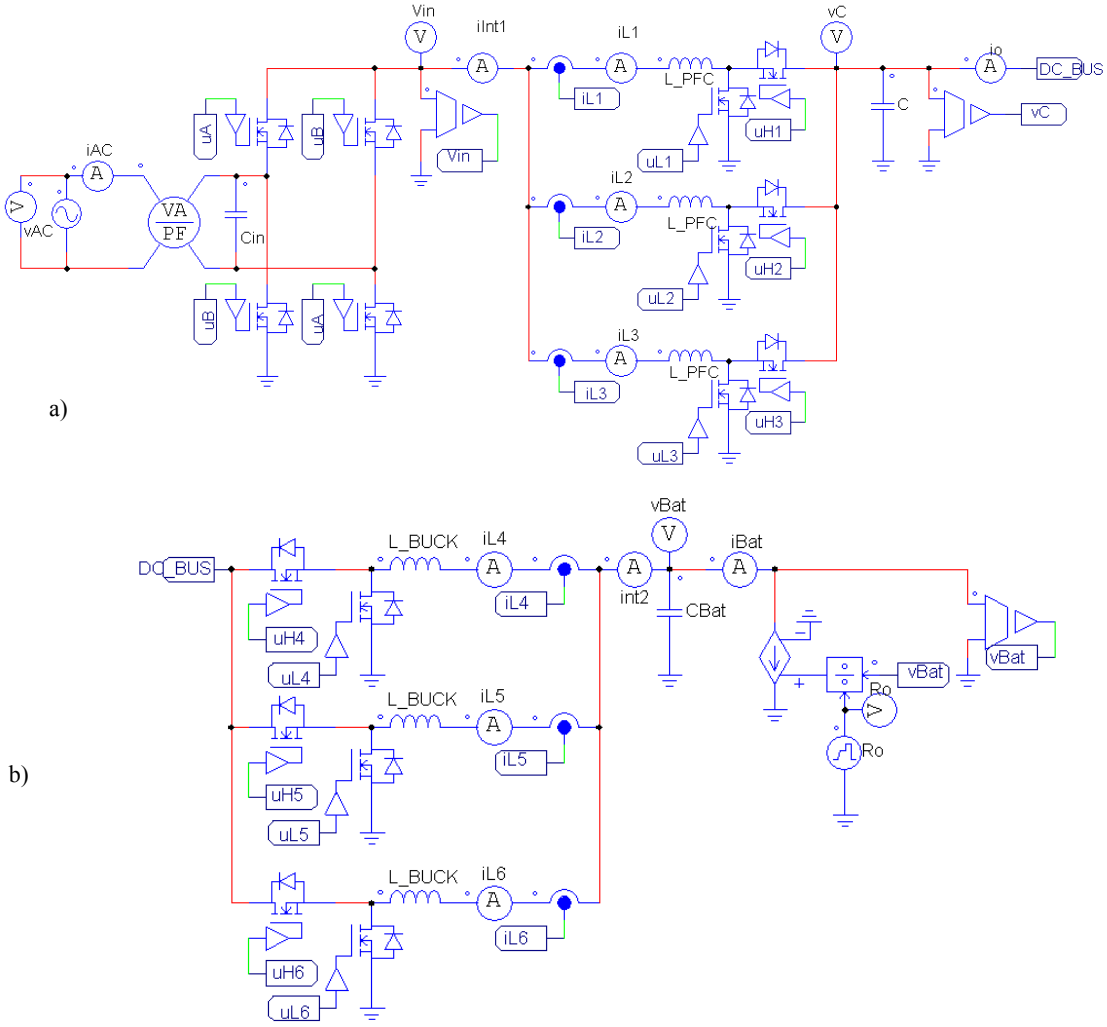


Fig. 5.1. PSIM model of the battery charger. a) Grid synchronised rectifier and PFC stage. b) BCR stage and emulated battery as a variable R_o.

All six inductor current controllers have been simulated by means of submodules. In particular Fig. 5.3.a illustrates the submodules that correspond to the inductor current controllers of the PFC stage. These controllers have in common the inductance value of the PFC cells, the switching period ($1/f_{SW}$), the PFC inductor current reference, the samples of the DC-link and rectified input voltage. However, each controller receives the samples of a different inductor current, as well as a different synchronisation and saw tooth signals. It is possible to see in Fig. 5.3.b that the simulated current-mode controller corresponds to the equivalent control for the average current-mode type of control for a boost converter $\tau_{eq,j}^{n}$ which can be found in Table 4.2. Note that the resulting duty cycle has been saturated between 0.15 and 0.99. The minimum duty cycle has been adjusted considering that the PFC inductor current controller execution is

finished in 2.5 µs since the beginning of the switching period, while the maximum duty cycle has been adjusted experimentally.

The DC-link voltage regulation loop is depicted in Fig. 5.4. Constant parameters z_o, k_p, a_1, a_2 and b_1 are defined in Table 4.5. Note that one synchronisation signal of f_{S2}=10 kHz is used to trigger the computation of the new value of conductance G^n and all unit delays depend on frequency f_{S2}. Last sample & hold block of the chain is used to simulate the moment in which the new value of $g^n = 1/3 \cdot G^n$ is ready to be used according to the sequence execution commented previously. The PFC inductor current reference is computed as the multiplication of g^n and the rectified input voltage sample v_{in}^n, and the result is ready to be used at the beginning of the switching period of the second cell of the PFC stage.

Similarly to the PFC case, BCR inductor current controllers share some information, such as, the current reference, switching period T_{SW}, inductance value and the sampled battery and DC-link voltages. However, each controller receives different synchronisation signals and the sampled inductor current value from its corresponding buck converter (see Fig. 5.5.a). In this case, the control law that has been simulated corresponds to $\tau_{eq,i}^n$ of Table 4.2 for the average type of control for buck converters. The resulting duty cycle has been limited between 0.5 and 0.99 in this case.

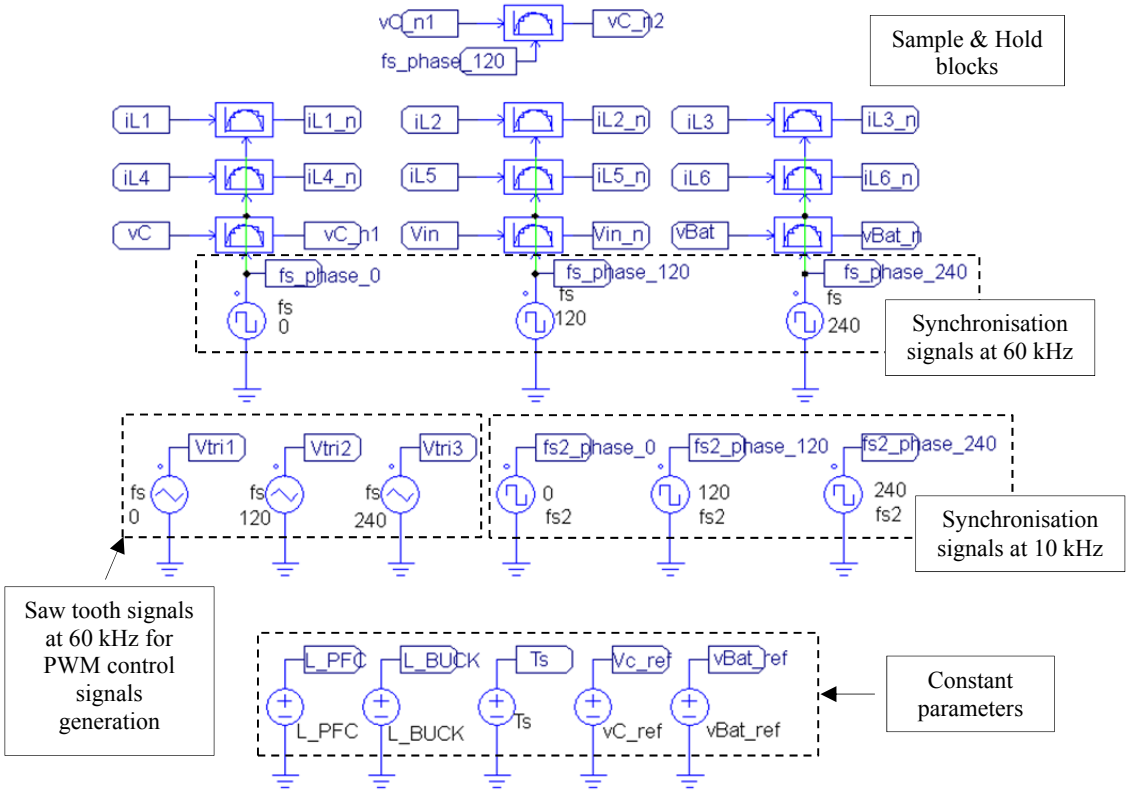
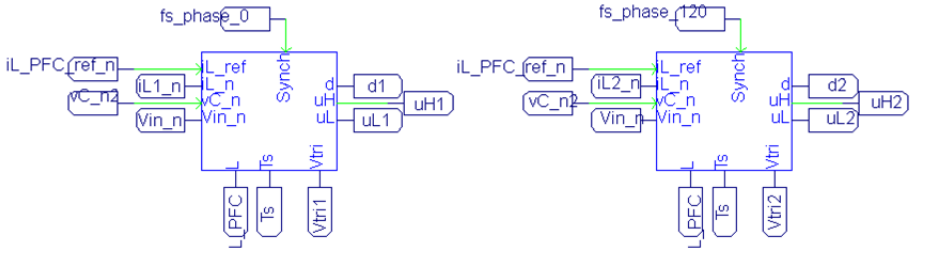


Fig. 5.2. Synchronisation signals, sample & hold blocks for ADC emulation, triangular waveforms for PWM control signals generation and constant parameters.

a)



b)

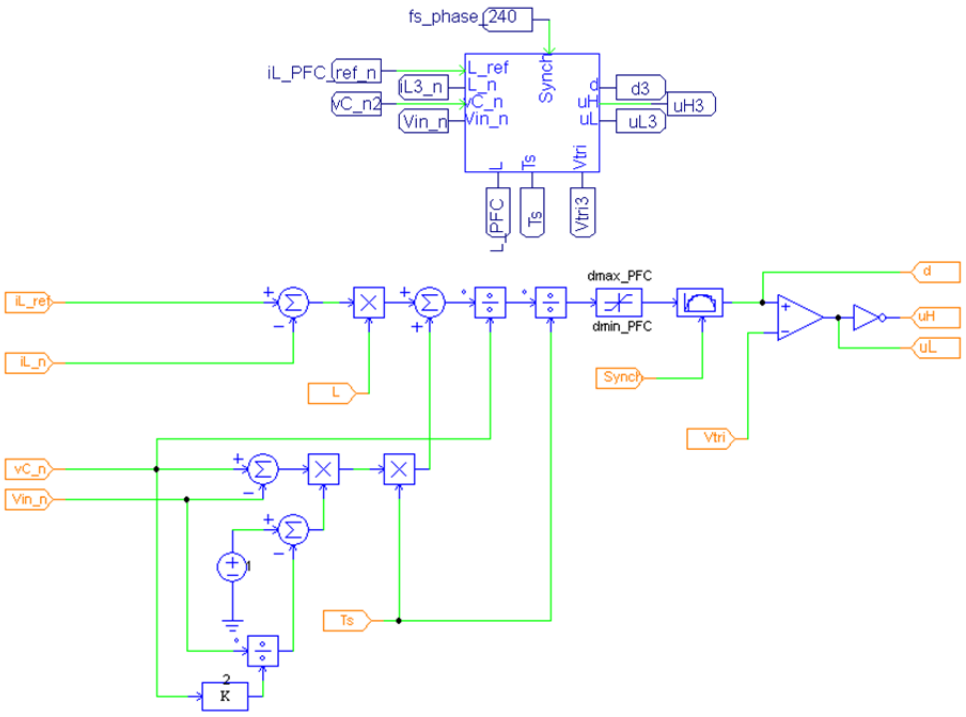
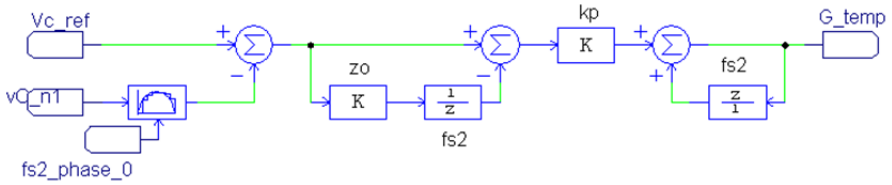
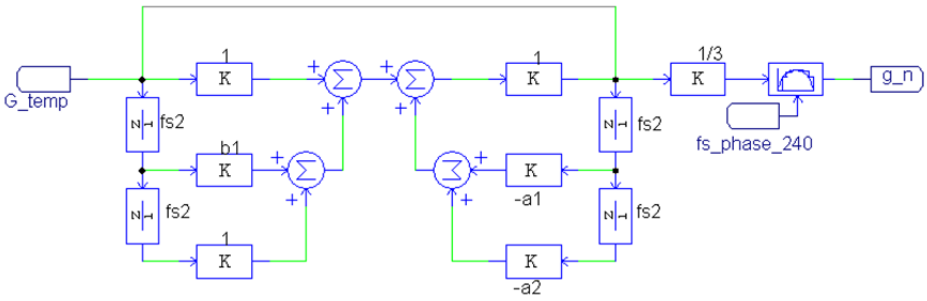


Fig. 5.3. a) Submodules of the three PFC inductor current controllers. b) Content of the submodules.

a)



b)



c)

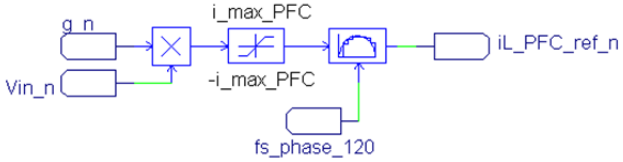


Fig. 5.4. a) PI DC-link voltage controller. b) Notch filter. c) PFC inductor current reference calculation.

Inductor current reference of buck converters is provided by the battery voltage controller depicted in Fig. 5.6. Similarly to the DC-link voltage regulation loop, the battery voltage controller depends on a synchronisation signal of 10 kHz and constant parameters z_{oBat} and k_{pBat}, which have been previously defined in section 4.4. The battery current reference is limited at a maximum value of 8 A to impose the CC operation mode. Then, inductor current reference is calculated as one third of the battery current reference. The last sample & hold block is employed to update new current reference at the beginning of the next execution sequence.

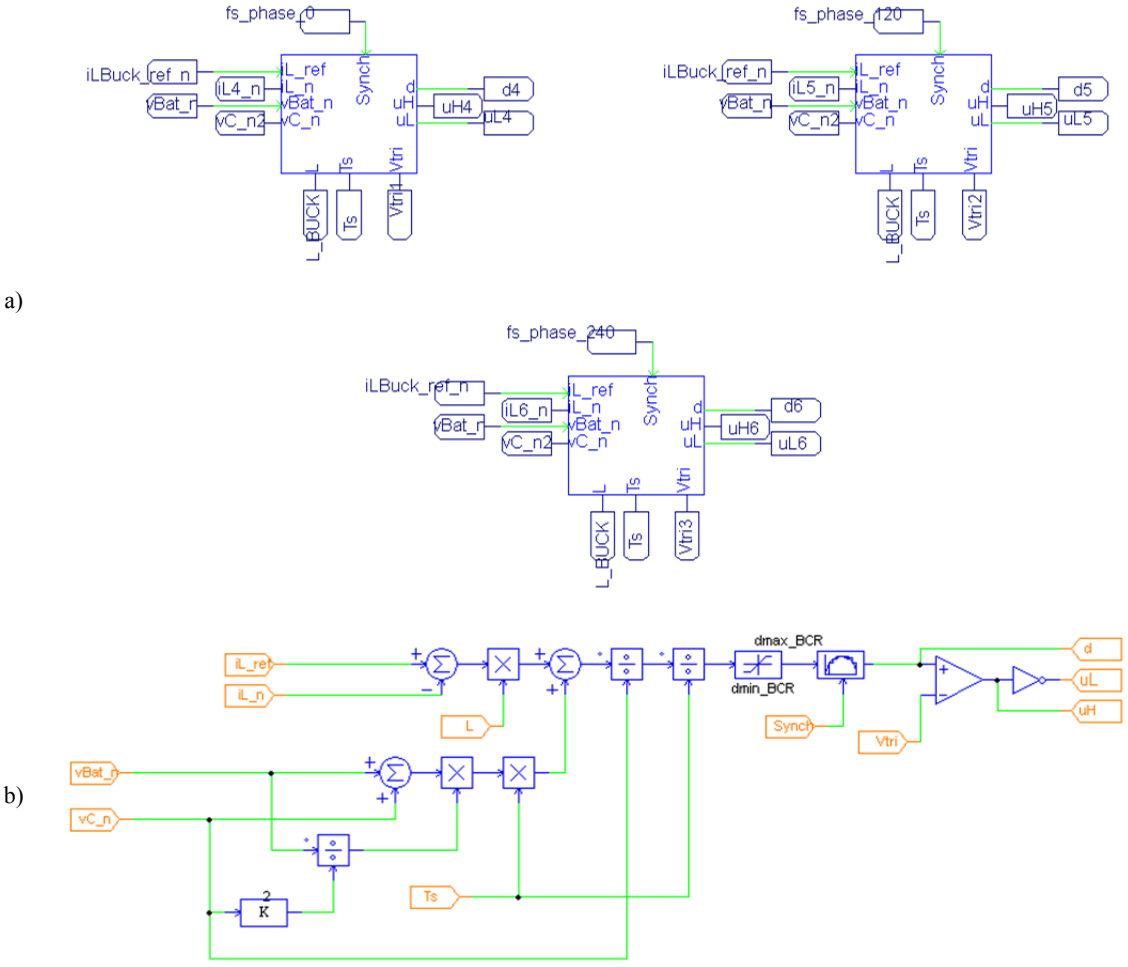


Fig. 5.5. a) Submodules of the three inductor current controllers for the BCR stage. b) Content of the submodules.

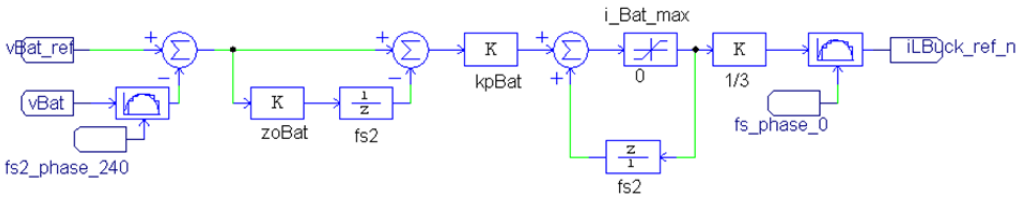


Fig. 5.6. PI battery voltage controller.

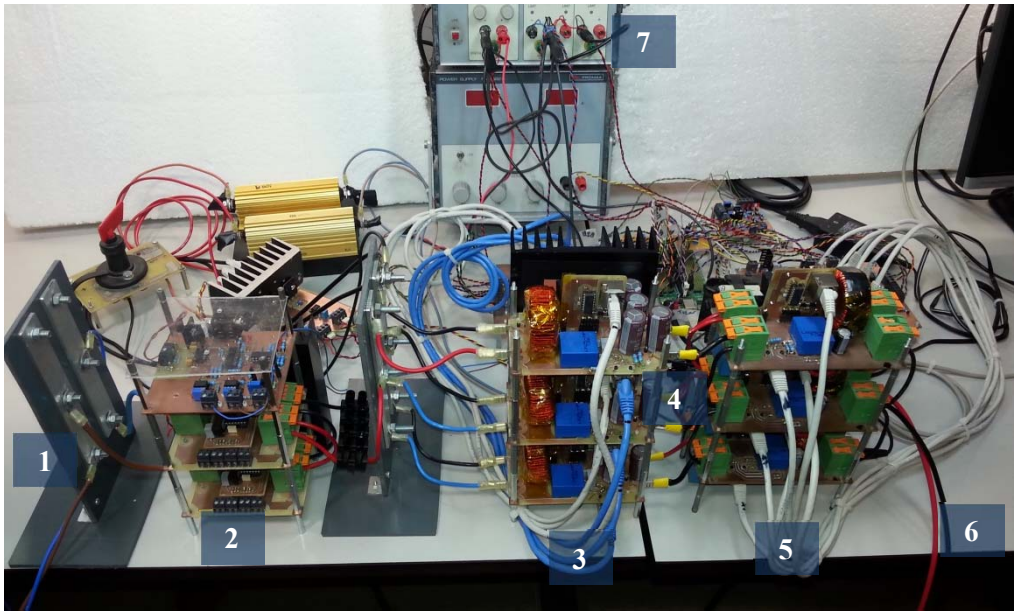
5.2 Experimental set-up

5.2.1 Implemented prototype

Two different perspectives of the implemented prototype are illustrated in Fig. 5.7. The main parts of the prototype are listed below.

1. Connection to an AC power source.
2. Grid-synchronised rectifier.

a)



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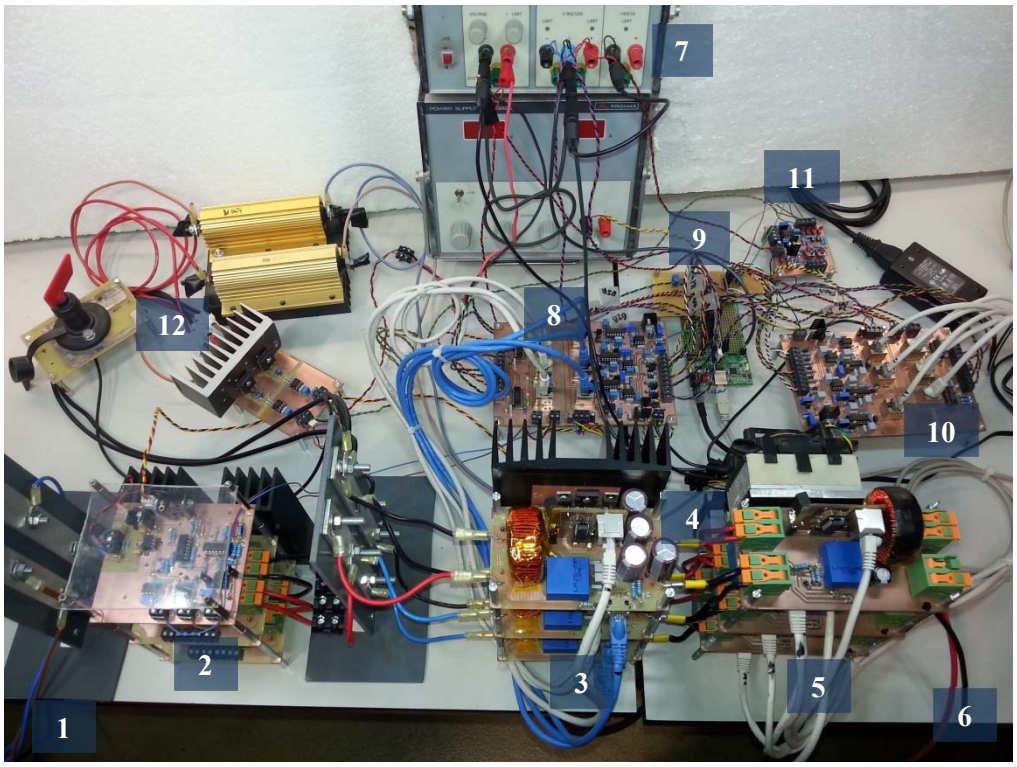


Fig. 5.7. Experimental set-up for testing of the implemented prototype. a) General view. b) Top view.

3. Three boost converters of the PFC stage.
4. DC-link connection.
5. Three buck converters of the BCR stage.
6. Connection to an electronic load.
7. Power supply for the sensing and driving circuitry.
8. Interconnection board between the PFC stage and the DSC.
9. C2000 experimenter kit based on a TMS320F28335 DSC from TEXAS INSTRUMENTS.
10. Interconnection board between the BCR stage and the DSC.
11. User control switches.
12. Resistors for discharging the DC-link and electronic load connections in case of overvoltage conditions. One MOSFET connects each 100 Ω power resistor to the ground if the DC-link voltage surpasses the level 450 V or the output voltage surpasses the 400 V. The rotatory switch is employed to force the discharge of the DC-link capacitors manually if required.

5.2.2 Laboratory equipment

The most important laboratory equipment that has been used to carry out the experimental results is included in the following list.

1. A 360-AMX AC power source from PACIFIC POWER SOURCE to emulate the grid.
2. An EA-EL 9750-75 HP electronic load from ELEKTRO – AUTOMATIK has been configured in resistive mode to emulate the SoC of the battery. It has been controlled externally with a function generator to vary the load resistance.
3. An AFG2021 function generator from TEKTRONIX to vary the resistance of the power load.
4. A WT3000 power analyser from YOKOWAGA to measure the low-frequency harmonics, THD and PF of the system.
5. A FAC-363B power supply from PROMAX to supply the sensing and driving circuitry.
6. A MCO3014 oscilloscope from TEKTRONIX to capture most of the oscilloscope figures.
7. A DLM4038 oscilloscope from YOKOWAGA to capture Fig. 4.13.
8. TCP0020 current probes from TEKTRONIX.
9. THDP0200 high voltage differential probes from TEKTRONIX.

5.3 Grid-to-Vehicle operation

Simulation and experimental results that are firstly reported in this chapter correspond to the Grid-to-Vehicle operation of the battery charger. Fig. 5.8 illustrates the steady-state operation of the battery charger under maximum load conditions in case of not using the Notch filter in the DC-link voltage regulation loop. In particular it depicts the absorbed line current $i_{AC}(t)$, line voltage $v_{AC}(t)$, the DC-link voltage $v_C(t)$ and battery voltage $v_{Bat}(t)$. As it can be observed, AC variables are correctly in phase. However, the absence of the Notch filter produces an important distortion of $i_{AC}(t)$, so that the PFC stage is not capable to achieve a unity PF. This distortion is mainly produced by the high amplitude of the third harmonic of $i_{AC}(t)$, this resulting in a relatively high THD. Apart from that, it is possible to see how the DC-link voltage is correctly regulated at 400 V_{DC} and the battery voltage is 380 V.

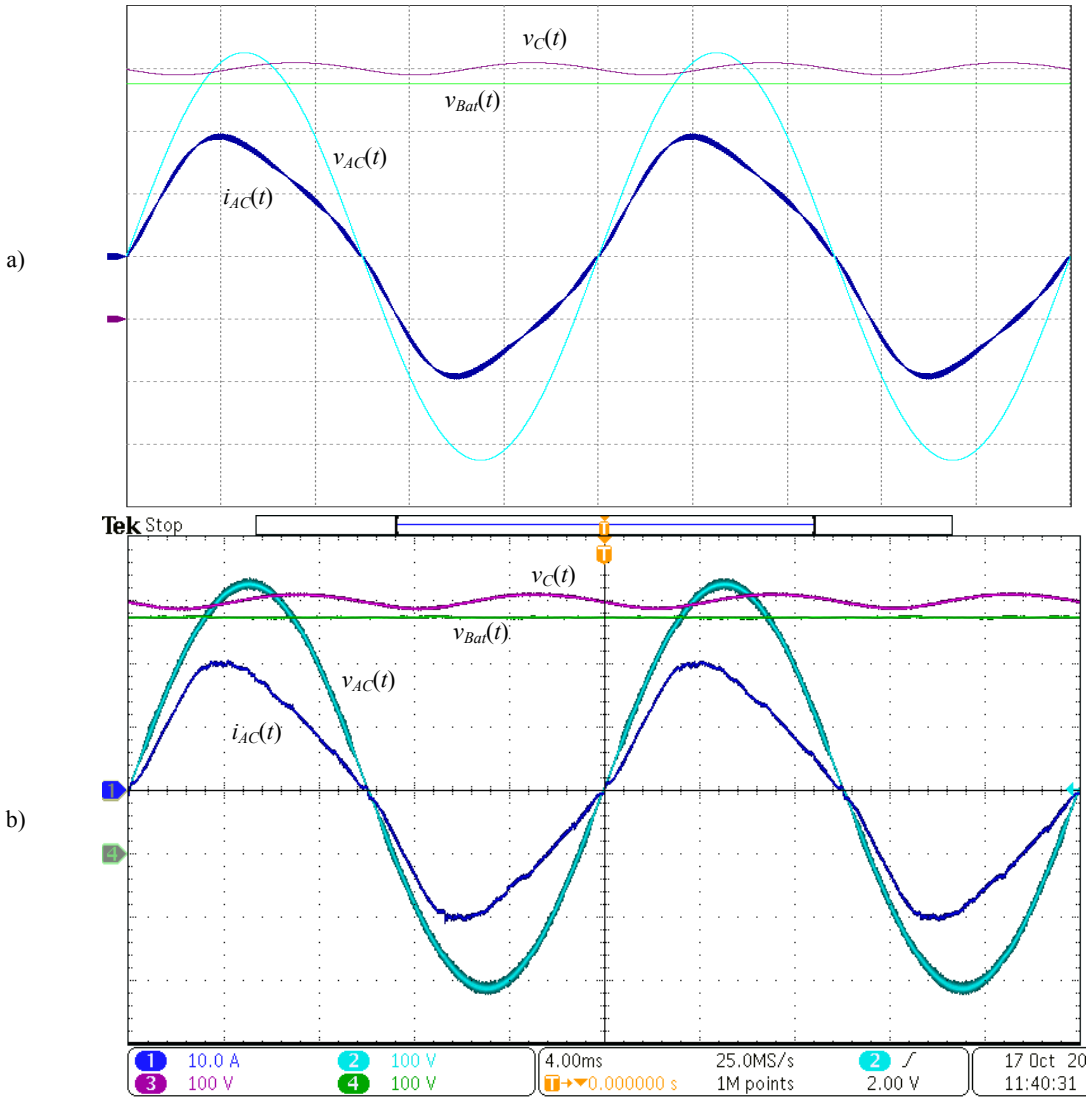
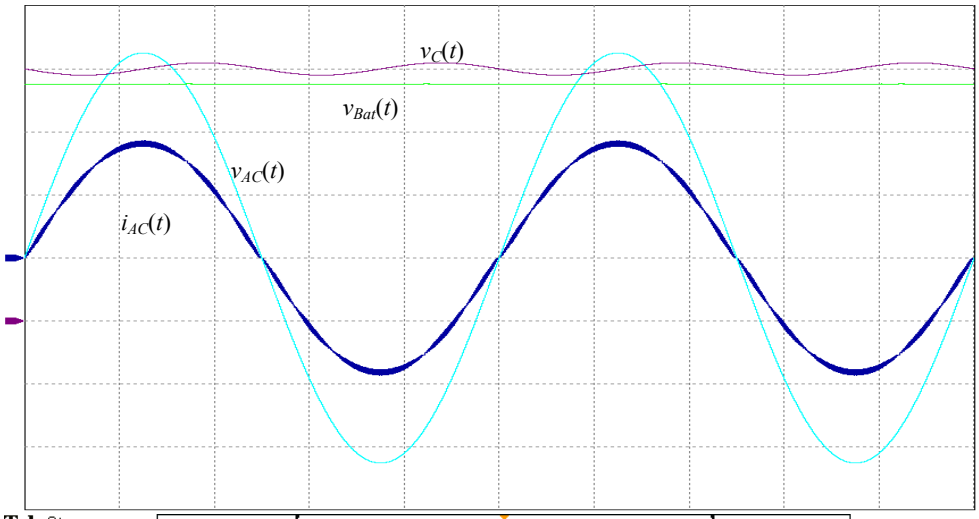


Fig. 5.8. Steady-state operation of the battery charger under maximum load conditions and without using the Notch filter (4 ms/div). CH1: line current $i_{AC}(t)$ (10 A/div). CH2: line voltage $v_{AC}(t)$ (100 V/div). CH3: DC-link voltage $v_C(t)$ (100 V/div). CH4: battery voltage v_{Bat} (100 V/div). a) Simulation. b) Experimental result.

a)



b)

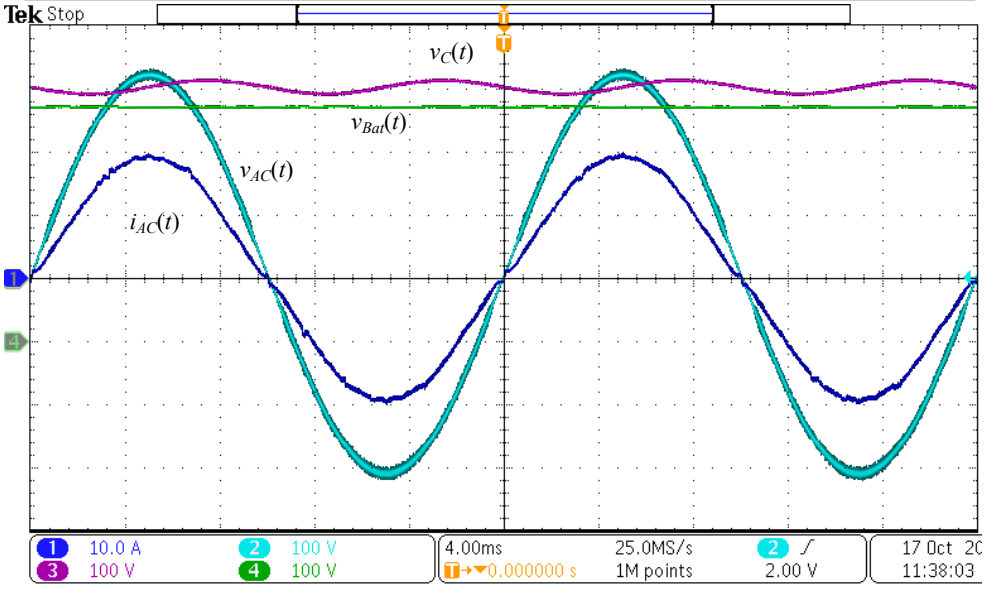


Fig. 5.9. Steady-state operation of the battery charger under maximum load conditions and using the Notch filter (4 ms/div). CH1: $i_{AC}(t)$ (10 A/div). CH2: $v_{AC}(t)$ (100 V/div). CH3: $v_C(t)$ (100 V/div). CH4: v_{Bat} (100 V/div). a) Simulation. b) Experimental result.

In contrast, the third harmonic distortion of line current is importantly mitigated in Fig. 5.9 due to the application of the Notch filter. Therefore, it can be affirmed that in this case the PFC stage is better emulating the behaviour of an LFR than in the previous case because the proportionality between the line voltage and current is more constant.

Besides, Fig. 5.10 demonstrates the correct interleaving operation of PFC stage inductor currents. As it can be seen, this operation results in a ripple cancelation effect on current $i_{INT1}(t)$ in addition to an increment of its effective switching frequency to $3 \cdot f_{SW}$ as expected. Remember that $i_{INT1}(t)$ is defined as the sum of the three inductor currents of the PFC stage.

5. Simulation and experimental results

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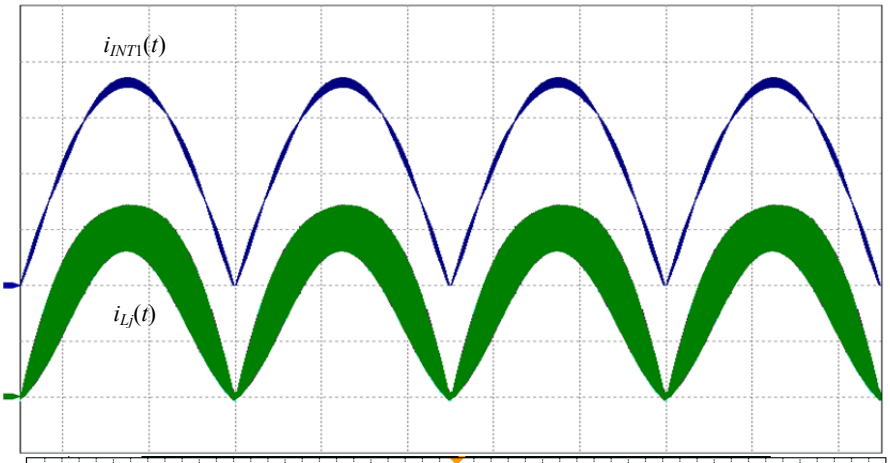

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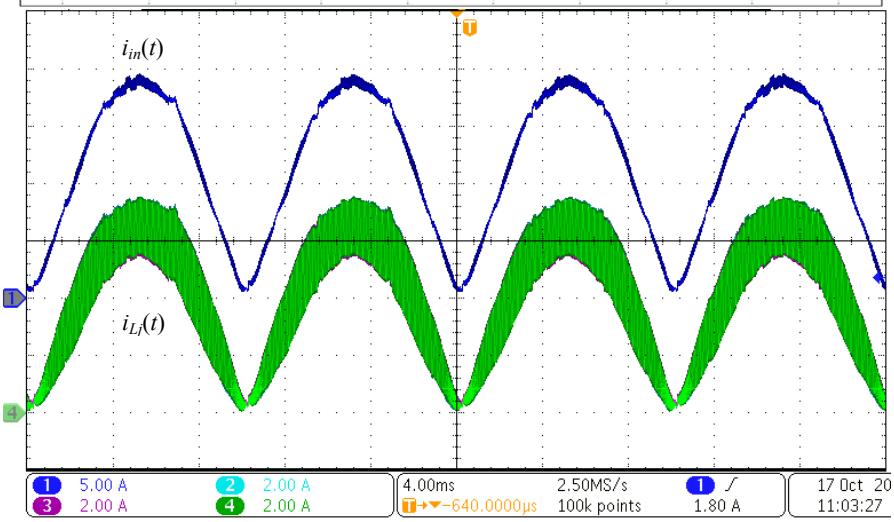

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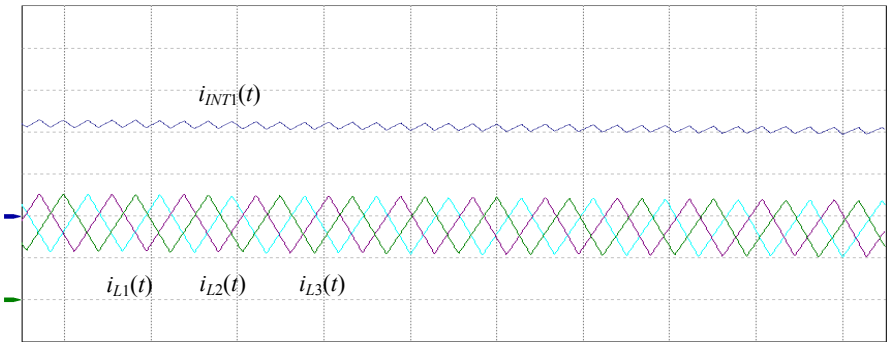

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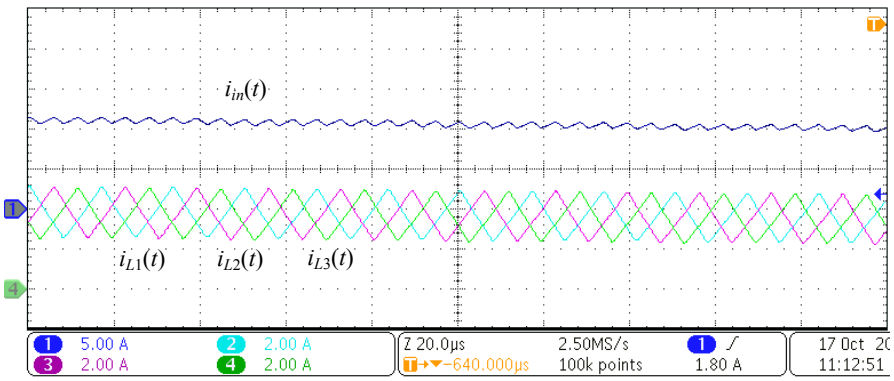

Fig. 5.10. Currents from the PFC stage. CH1: $i_{INT1}(t)$ (5 A/div). CH2: $i_{L1}(t)$ (2 A/div). CH3: $i_{L2}(t)$ (2 A/div). CH4: i_{L3} (2 A/div). a) Simulation, b) experimental result (4 ms/div). Zoom c) simulation, d) experimental result (20 µs/div).

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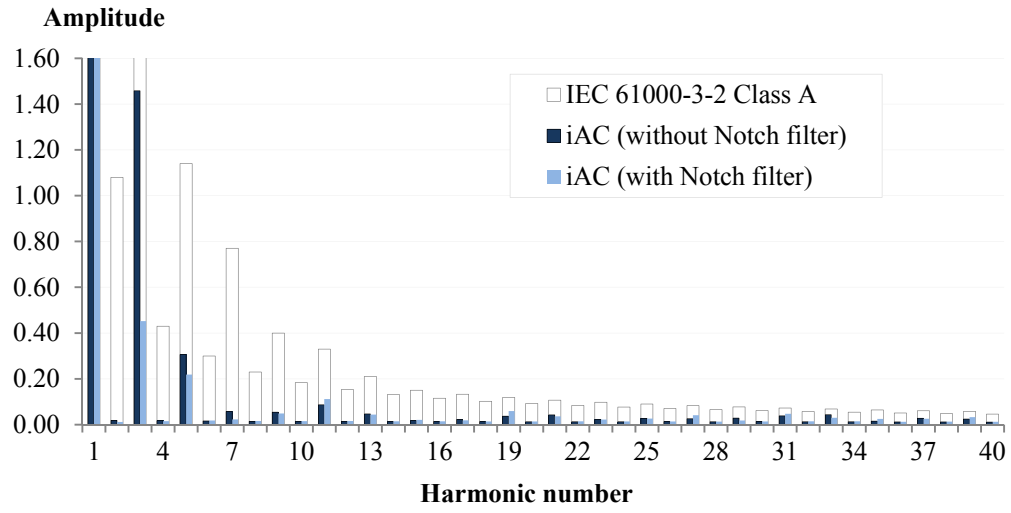

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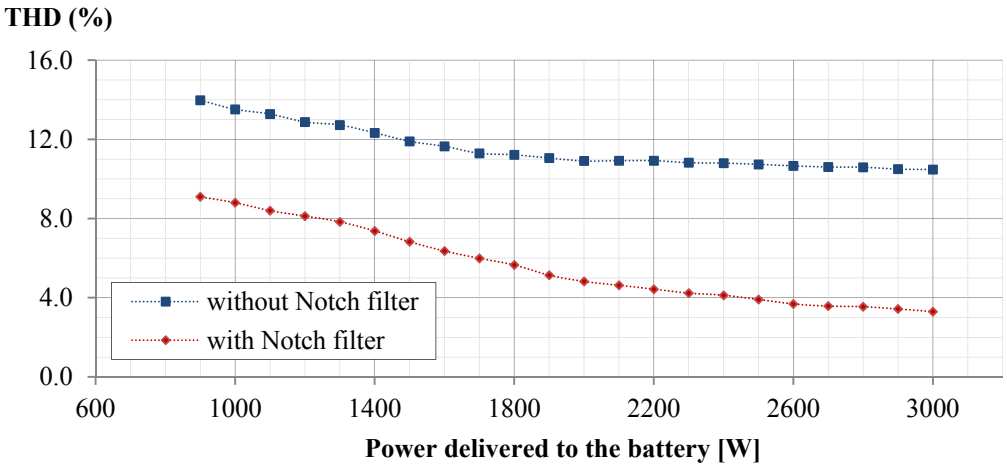

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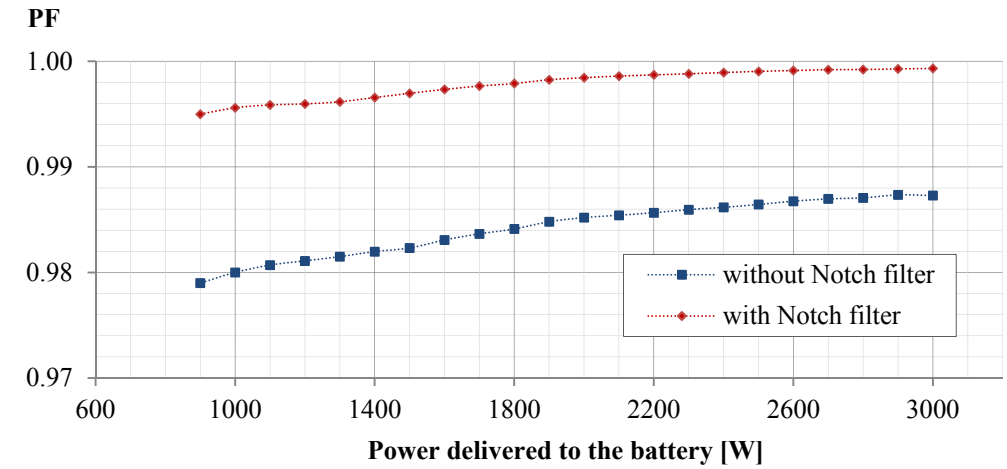


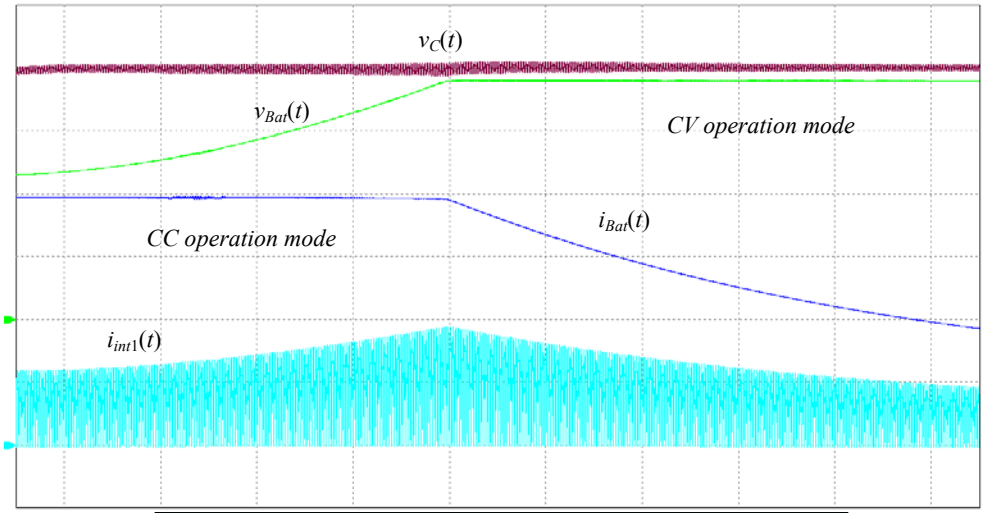
Fig. 5.11. Measured a) low-frequency harmonic spectrum of line current $i_{AC}(t)$ under maximum load conditions, b) total harmonic distortion (THD), c) power factor (PF).

The PFC performance of the battery charger is illustrated in Fig. 5.11. It is important to remark that all measures have been obtained for a DC-link voltage value of 400 V_{DC}. Fig. 5.11.a depicts how the low-frequency harmonics of $i_{AC}(t)$ for maximum load conditions are in agreement with standard IEC 61000-3-2 for Class A equipment. However, the amplitude of the third harmonic

is clearly higher when the Notch filter is disabled. For that reason, the system exhibits a higher THD and lower PF as depicted in Fig. 5.11.b and Fig. 5.11.c respectively. As it can be also observed, the best power factor correction performance corresponds to the maximum load conditions in which the system achieves a THD of 3.3 % approximately and a PF very close to the unity when the Notch filter is activated.

Next simulation and experimental results correspond to the emulated battery charging profile. Although in a real application the battery charging would last several hours, the charging operation has been temporally scaled to only 4 seconds to illustrate it in a single figure (see Fig. 5.12). As it can be seen, the battery charger operates in both CC and CV operation modes. CC operation mode corresponds to the time while the battery current is saturated slightly below the 8 A since the battery voltage is lower than 380 V. Once this level of voltage is achieved, the

a)



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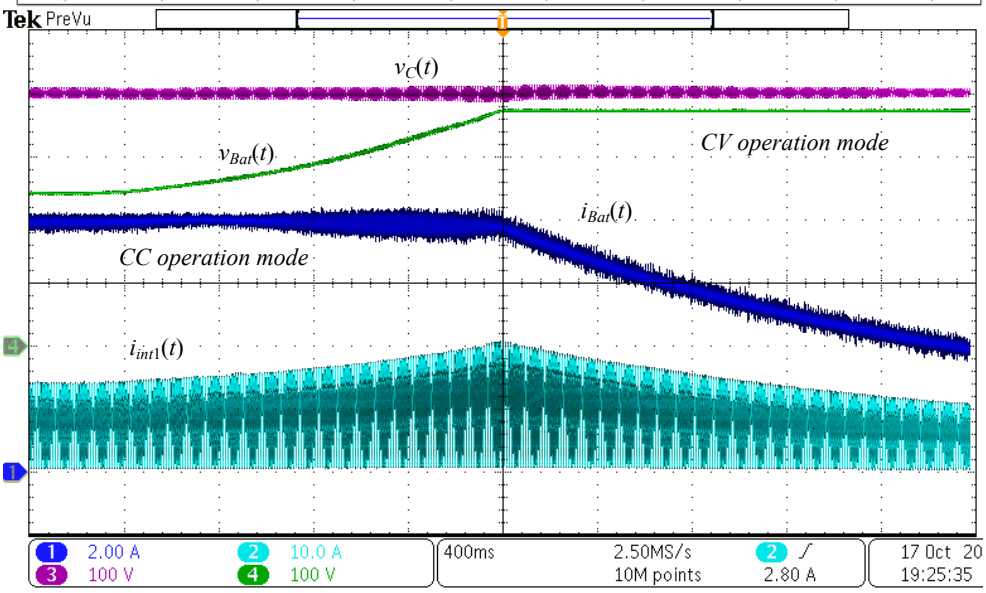

Fig. 5.12. Battery charging emulation with CC-CV operation mode transition (400 ms/div). CH1: $i_{Bat}(t)$ (2 A/div). CH2: $i_{int1}(t)$ (10 A/div). CH3: $v_C(t)$ (100 V/div). CH4: v_{Bat} (100 V/div). a) Simulation. b) Experimental result.

battery charger starts working in CV operation mode and the battery current is decreased progressively with the increase of the output resistance that emulates the charge of the battery. It has to be commented that at the beginning of the sequence visible in Fig. 5.12.b R_o presents a resistance of 30 Ω while at the end it is around 100 Ω. It is also interesting to note that the DC-link voltage is correctly regulated at 400 V_{DC} for the whole operation. Finally, it is easy to deduce that the battery charger reaches the maximum load conditions at the end of the CC operation mode because the multiplication of the battery voltage and the battery current reaches its maximum value. Similarly, current $i_{INT1}(t)$ reaches its maximum value at this point and DC-link voltage also presents its maximum voltage ripple. A minor detail is that the battery current exhibits a higher ripple in the experimental results than in the simulation. This is because the battery was modelled as a voltage controlled current source in the simulation.

Finally, Fig. 5.13.a illustrates the evolution of inductors' currents and battery current for the same charging operation profile illustrated in the previous figure. Note that during the CC operation mode, the average value of inductors' current is maintained constant and it starts to decrease when the CV operation mode is started. It is also interesting to note that the ripple of inductors' current exhibits the highest width when the battery voltage is lowest and, as expected, the ripple decreases progressively as long as the battery voltage increases. Once the CV operation mode is started, the inductors' current ripple remains constant since the battery voltage is regulated at 380 V. What is more, the interleaving operation of inductor currents of the BCR stage is depicted in Fig. 5.13.c and Fig. 5.13.d. They present a correct phase-shift of 120º and a proper current sharing between the three buck cells. As well as in the PFC stage, the sum of the three inductor currents results in a ripple cancellation effect and an effective switching frequency of three times the original switching frequency.

5.4 Vehicle-to-Grid operation

This section includes the simulation results on the Vehicle-to-Grid operation of the battery charger. In particular, the steady-state operation under maximum load conditions is illustrated in Fig. 5.14. As it can be observed line current and line voltage have opposite sign, which means that line current is injected to grid. Battery voltage value is 380 V, the DC-link voltage is regulated at 400 V_{DC} and line current has a peak value of 20 A approximately, similarly to the Grid-to-Vehicle operation reported previously. It is also important to highlight that the system is expected to achieve a high PF because line current and line voltage are proportional and in phase correctly.

5. Simulation and experimental results

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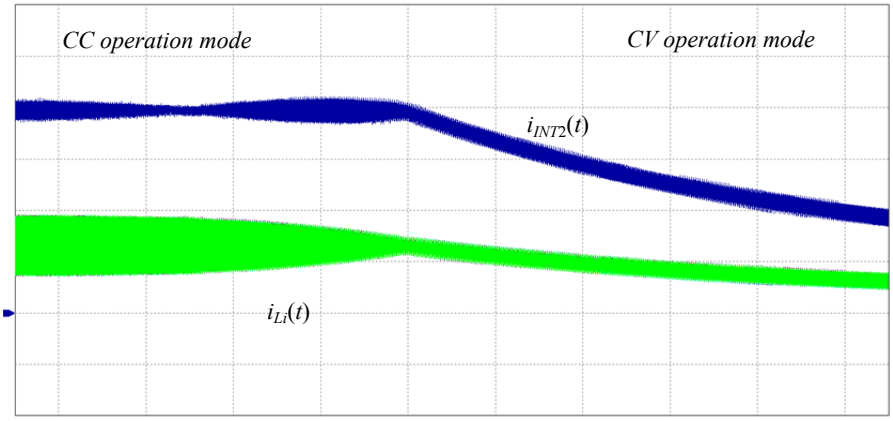

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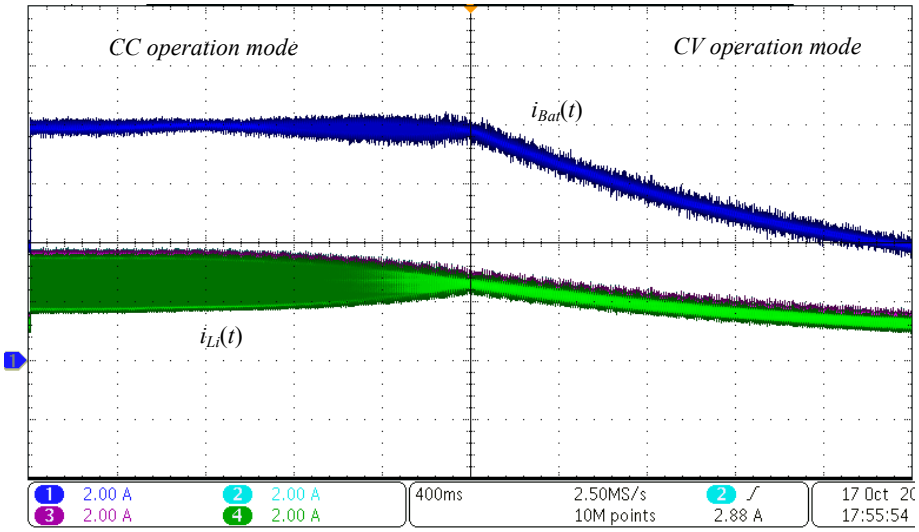

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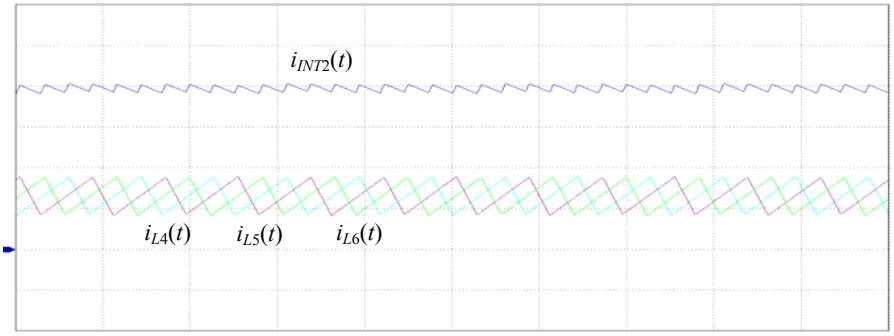

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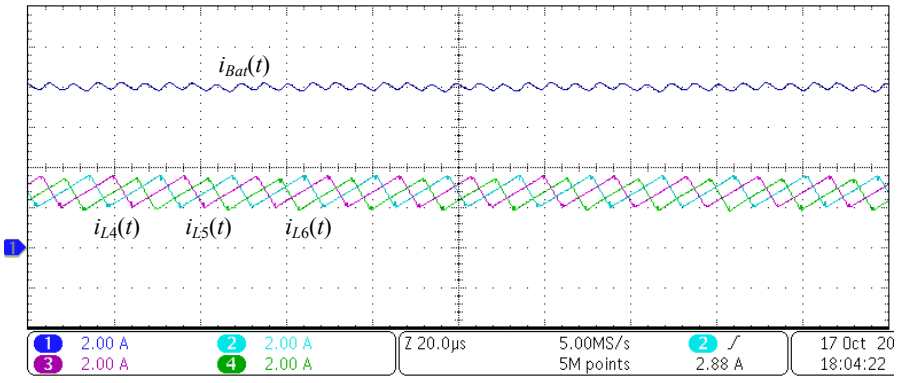


Fig. 5.13. Currents in the BCR stage. CH1: $i_{Bat}(t)$ (2 A/div). CH2: $i_{L4}(t)$ (2 A/div). CH3: $i_{L5}(t)$ (2 A/div). CH4: i_{L6} (2 A/div). a) Simulation, b) experimental result (400 ms/div). Zoom c) simulation, d) experimental result (20 µs/div).

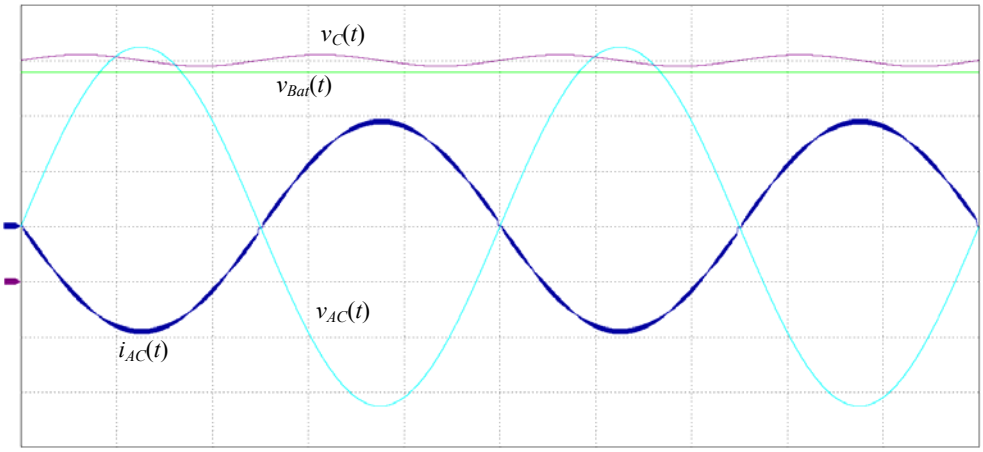


Fig. 5.14. Simulation result of the steady-state operation of the battery charger under maximum load conditions for Vehicle-to-Grid operation (4 ms/div). CH1: $i_{AC}(t)$ (10 A/div). CH2: $v_{AC}(t)$ (100 V/div). CH3: $v_C(t)$ (100 V/div). CH4: v_{Bat} (100 V/div).

5.5 Conclusions and future work

First part of this chapter describes how the battery charger has been modelled and simulated by means of the PSIM package. The rest of the chapter corresponds to the different simulation and experimental results of the proposed and implemented 3 kW digitally controlled battery charger.

The LFR behaviour of the first stage of the battery charger has been demonstrated since line current and line voltage are proportional and in phase. It has also been demonstrated that the DC-link voltage was correctly regulated at 400 V_{DC} and that the use of the Notch filter reduces the third harmonic amplitude of line current and, in consequence, improves the PFC performance of the first stage. The measured PF and THD at 3 kW load conditions are 0.99933 and 3.30 % respectively.

Moreover, both CC and CV operation modes of the battery charger have been validated experimentally. In particular, 8 A were supplied to the load for the CC operation mode and 380 V were regulated during the CV operation mode.

Although only grid-to-vehicle experimental results have been reported, vehicle-to-grid experimental results are in progress to demonstrate that the proposed battery charger can operate in both directions of the power flow as illustrated by simulation in Fig. 5.14. A future work would also include the design a specific BMS for testing the battery charger operation with a real battery, and the design an EMI filter to comply with the corresponding standards.

UNIVERSITAT ROVIRA I VIRGILI
DESIGN AND CONTROL OF A BATTERY CHARGER FOR ELECTRIC VEHICLES
Adrià Marcos Pastor

Chapter 6

DC-LINK CAPACITANCE REDUCTION

This chapter analyses the reduction of the DC-link capacitance that is generally present in most of two-stage-based plug-in battery chargers. The proposed reduction is achieved by means of a proper regulation of the DC-link voltage. In particular, two different scenarios will be analysed. The first one considers that the DC-link voltage is regulated by the PFC stage and the second stage behaves as a constant power sink. In contrast, the second scenario proposes the DC-link voltage regulation from the second stage. Despite the resulting limitations in each case, the achievable DC-link capacitance reduction is of high interest for substituting electrolytic capacitors for film capacitors.

6.1 Problem statement

Many single-phase AC-DC power conversion applications are based on two consecutive stages, a front-end switched-mode power converter to correct the PF, followed by a second converter that supplies the energy to the load as required (Fig. 6.1). Both stages are connected by the DC-link capacitor which is designed traditionally according to two specifications. One of them is the hold-up time, which is mandatory to be fulfilled if it is necessary to continue supplying energy to the second stage for a short time (10-20 ms typically) in case of a dropout of the line voltage. However, this specification would not be required in other applications in which a temporally switch-off of the system could be accepted, e.g. in battery charging applications. The other specification related to the DC-link capacitor design is its maximum voltage ripple, which is generally set very low (< 10% of $V_{C,RMS}$), this resulting in a sufficiently large capacitance that decouples both stages [110].

Traditionally, electrolytic capacitors have been employed as DC-link capacitors in high voltage applications owing to their smaller size with respect their capacity. However, their short lifespan has promoted their replacement for film capacitors in some applications, e.g. LED-based lightning [111] or battery chargers for EVs [112, 113]. For that reason, researchers from the industry and academia have focused on the reduction of the DC-link capacitance to develop more reliable high-density power converters. However, different issues derive from this reduction, e.g. it should not compromise the achievable PF or the THD of the PFC stage. This is why some approaches use additional converters to achieve an important DC-link capacitance

reduction, but at the expense of increasing the cost and complexity of the system. This is the case of [114], in which a bidirectional converter is added at the *AC* side of the system, while a simpler solution consists in connecting a bidirectional converter directly to the DC-link capacitor as in [115]. Other approaches are focused on the design of control strategies instead of increasing the number of components on the power stage in order to cope with low DC-link capacitances. One example is [112], which proposes the design of a PFC controller that is not affected by the high ripple of the DC-link voltage due to the low DC-link capacitance. A different control strategy is [116], in which the proposed DC-link capacitance reduction is achieved by means of the reduction of its voltage ripple. However, this technique increases the amplitude of line current low-frequency harmonics.

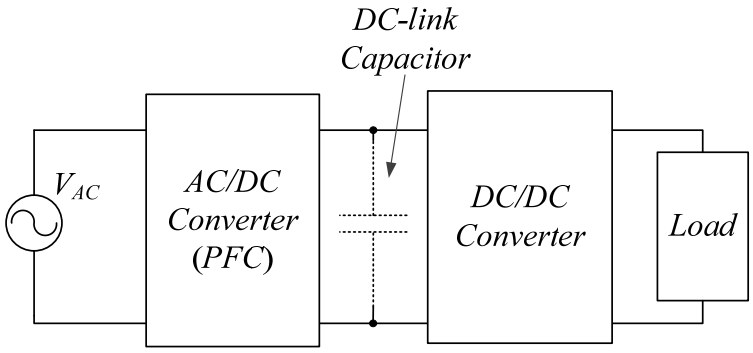


Fig. 6.1. General block diagram of a single-phase power supply system based on two cascaded stages and a DC-link capacitor.

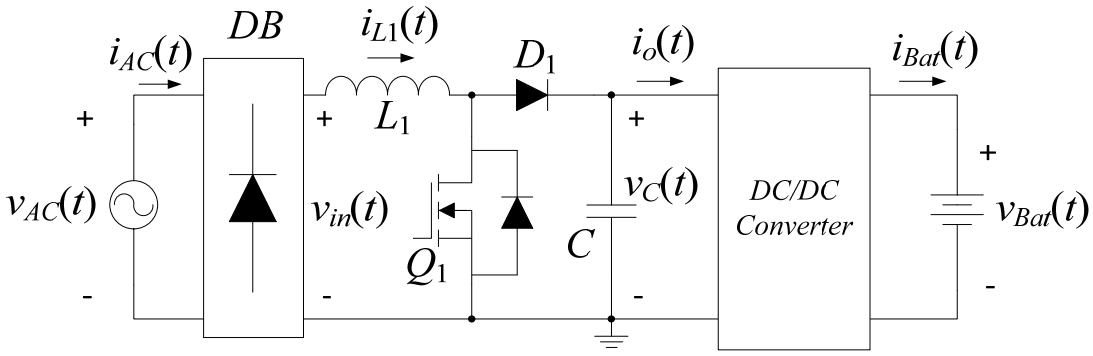


Fig. 6.2. PFC stage based on a boost converter and a diode bridge.

In this thesis, two different scenarios are analysed for achieving a high DC-link capacitance reduction. The first scenario considers that the second stage behaves as a constant power load and the DC-link voltage is regulated by the PFC stage, while the second scenario considers that the DC-link voltage is regulated by the second stage. Both scenarios have been analysed in the mark of battery charging applications that employ a conventional boost converter with a diode rectifier as the PFC stage (see Fig. 6.2). This implies that the DC-link voltage has to be always higher than the rectified input voltage for a proper operation.

Thus, this chapter is organised as follows. Section 6.2 presents the conventional design of the DC-link capacitance. Section 6.3 describes how to calculate the DC-link capacitor that forces the tangency between the rectified input voltage and the DC-link voltage. It also details the complete design of the PFC controller and includes different simulation and experimental. Besides, section 6.4 is focused on the DC-link voltage regulation from the second stage, which allows a further reduction of the DC-link capacitance. Finally, section 6.5 presents the conclusions of the chapter and future research lines.

6.2 Conventional design of the DC-link capacitor

This section presents how to derive the most employed formula in the industry to calculate the DC-link capacitance considering that the second stage of the system behaves as a constant power sink.

The first assumption is that the PFC stage behaves as an LFR. This implies that the ripple-free *AC* current $i_{AC}(t)$ is exactly in phase and proportional to voltage $v_{AC}(t)$, and all the absorbed input power P_{in} is transferred to the DC-link capacitor and to the power sink P_o. Hence, if the line voltage is defined as:

$$v_{AC}(t) = V_M \sin(\omega_o t) \tag{6.1}$$

where V_M and ω_o are the peak voltage and angular frequency of the line respectively, the input current is defined as follows:

$$i_{AC}(t) = \frac{v_{AC}(t)}{r} \tag{6.2}$$

where r stands for the emulated input resistance of the PFC stage. Remember that r can be also defined as $1/g$ where g stands for the emulated input conductance of the PFC stage. The line current can also be defined as:

$$i_{AC}(t) = I_M \sin(\omega_o t) \tag{6.3}$$

where I_M is the peak value of the line current. In addition, it can be deduced that I_M is equal to V_M/r. Both peak values are related with their corresponding *RMS* values as follows:

$$V_M = V_{AC,rms}\sqrt{2}; \quad I_M = I_{AC,rms}\sqrt{2} \tag{6.4}$$

The ideal waveforms of signals $i_{AC}(t)$, $v_{AC}(t)$ and $v_C(t)$ are depicted in Fig. 6.3. The absorbed input power is defined as follows:

$$P_{in} = v_{AC}(t) i_{AC}(t) = V_{AC,rms} I_{AC,rms} \left(1 - \cos(2\omega_o t)\right) = P_o + P_C \tag{6.5}$$

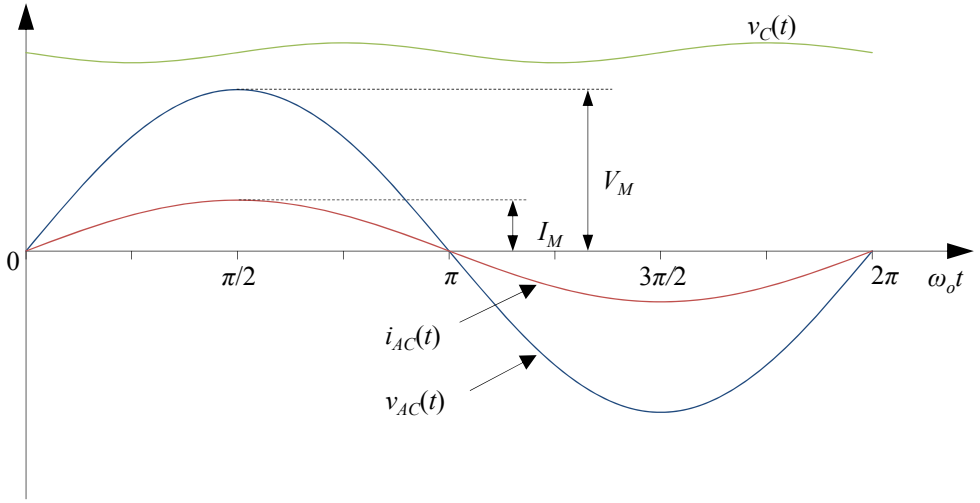


Fig. 6.3. Line voltage $v_{AC}(t)$, line current $i_{AC}(t)$ and DC-link capacitor voltage $v_C(t)$.

As it can be seen in equation (6.5), P_{in} contains a DC component and one harmonic at twice the line frequency. As it can be observed in Fig. 6.4, the DC component corresponds to power P_o whereas the harmonics corresponds to capacitor power P_C.

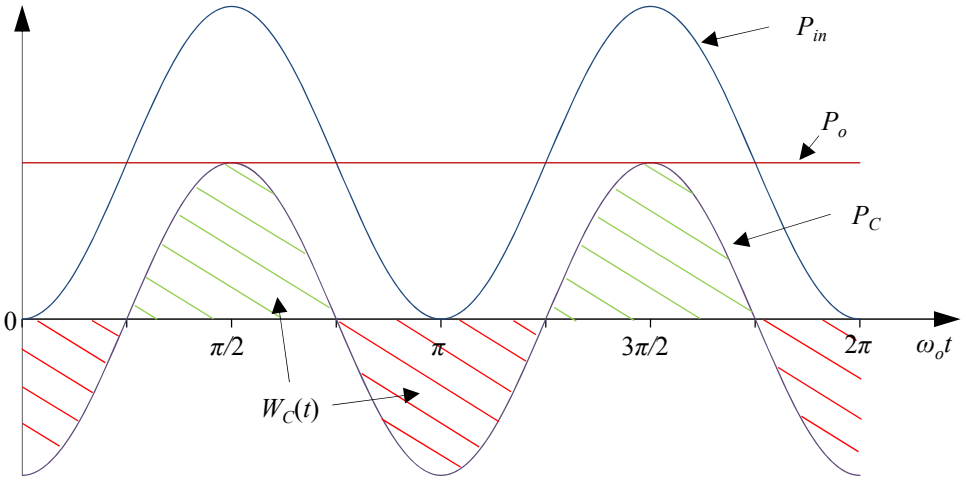


Fig. 6.4. Absorbed input power P_{in}, delivered output power P_o, capacitor power P_C and capacitor energy $W_C(t)$.

The DC component can be defined as:

$$P_o = V_{AC,rms} I_{AC,rms} \tag{6.6}$$

and

$$P_o = V_{C,rms} I_{o,rms} \tag{6.7}$$

where $V_{C,RMS}$ and $I_{o,RMS}$ correspond to the *RMS* values of $v_C(t)$ and $i_o(t)$ respectively. Hence, P_C is defined as follows:

$$P_C = -P_o \cos(2\omega_o t) \tag{6.8}$$

Note that P_C is positive when the DC-link capacitor is being charged whereas P_C is negative when the capacitor is delivering energy. Note also that the average value of P_C is 0 and, for that reason, it is considered that in steady-state P_{in}=P_o for one complete line period.

It is known that the stored energy in a capacitor is formulated as follows:

$$W_C(t) = \frac{1}{2} C v_C^2(t) \tag{6.9}$$

The energy of the capacitor is also defined by the following general expression:

$$W_C(t) = W_C(0) + \int_0^t P_C(\tau)\, d\tau \tag{6.10}$$

which results in:

$$W_C(t) = W_C(0) - \frac{P_o}{2\omega_o} \sin(2\omega_o t) \tag{6.11}$$

If $v_C(0)$=$V_{C,RMS}$ and equation (6.11) is used in (6.9), it results:

$$v_C(t) = V_{C,rms} \sqrt{1 - \frac{P_o}{C\omega_o V_{C,rms}^2} \sin(2\omega_o t)} \tag{6.12}$$

The minimum mathematical value for C which ensures a real solution to (6.12) is the following:

$$C_{\text{math}} = \frac{P_o}{\omega_o V_{C,rms}^2} \tag{6.13}$$

However, this value is not admissible in practice for a boost converter because it would generate a voltage waveform $v_{C=Cmath}(t)$, which is sometimes clearly lower than the rectified input voltage (see Fig. 6.5).

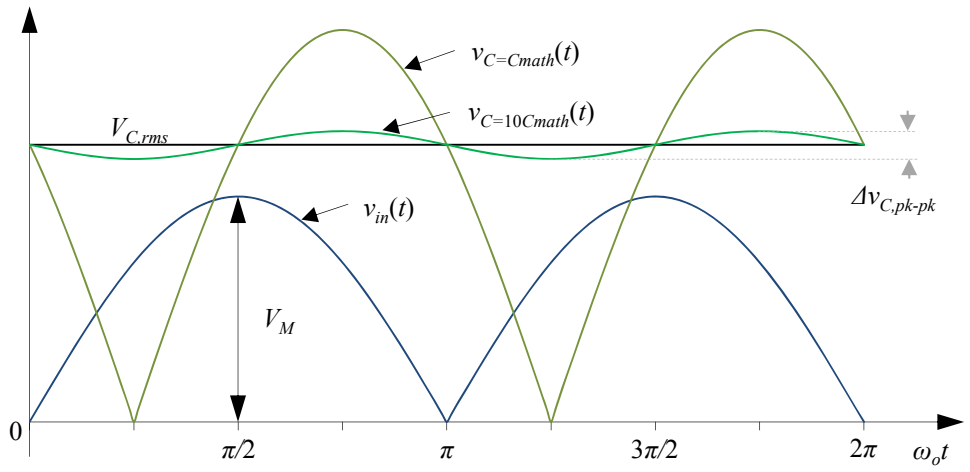


Fig. 6.5. Theoretical DC-link voltage waveforms for C=C_{math}, C=10C_{math} and rectified input voltage $v_{in}(t)$.

Moreover, the minimum and the maximum values of the DC-link voltage are achieved at $t_1=\pi/(4\omega_o)$ and $t_2=3\pi/(4\omega_o)$ respectively for any DC-link capacitor value. Hence:

$$v_{C,\min} = v_C(t_1); \quad v_{C,\max} = v_C(t_2) \tag{6.14}$$

Therefore, the capacitor energy at $t=t_2$ with respect $t=t_1$ is:

$$W_C(t_2) = W_C(t_1) + \int_{t_1}^{t_2} -P_o \cos(2\omega_o \tau)\, d\tau \tag{6.15}$$

Then, the following expression is obtained:

$$\frac{1}{2} C v_{C,\max}^2 = \frac{1}{2} C v_{C,\min}^2 + \frac{P_o}{\omega_o} \tag{6.16}$$

So that, the necessary capacitor can be calculated by using the following expression:

$$C = \frac{2P_o}{\omega_o \left(v_{C,\max}^2 - v_{C,\min}^2 \right)} \tag{6.17}$$

If maximum and minimum voltages of $v_C(t)$ were provided by the design specifications, equation (6.17) must be used to design the DC-link capacitor. However, these two values are not generally indicated and it is more common to have $V_{C,RMS}$ and the desired relative peak-to-peak voltage ripple $\Delta v_{C,pk\text{-}pk}$ (%) instead. This factor is defined as $\Delta v_{C,pk\text{-}pk}/V_{C,RMS}$ where $\Delta v_{C,pk\text{-}pk}$ is the peak-to-peak voltage ripple of $v_C(t)$. In case of having a capacitor sufficiently large, i.e. $C>4C_{math}$, it is possible to define the following approximations:

$$\begin{aligned} v_{C,\min} &\approx V_{C,rms} - \Delta v_{C,pk} \\ v_{C,\max} &\approx V_{C,rms} + \Delta v_{C,pk} \end{aligned} \tag{6.18}$$

where $\Delta v_{C,pk}=\Delta v_{C,pk\text{-}pk}/2$. Using (6.18) in equation (6.17) results in the conventional DC-link capacitor design C_{conv}:

$$C_{conv} = \frac{P_o}{2\omega_o \Delta v_{C,pk} V_{C,rms}} \tag{6.19}$$

or

$$C_{conv} = \frac{P_{o,\max}}{\omega_o V_{C,rms}{}^2 \Delta v_{C,\mathrm{pk-pk}}(\%)} \tag{6.20}$$

Equation (6.20) is the conventional expression to design the necessary DC-link capacitor in order to have a peak-to-peak voltage ripple relatively low, i.e. $\Delta v_{C,pk\text{-}pk}(\%)<10$ %. For example, $v_{C=10Cmath}(t)$ in Fig. 6.5 corresponds to a $\Delta v_{C,pk\text{-}pk}(\%)=10$ %. It is important to remark that the capacitor has to be designed according to the maximum power operation of the system ($P_{o,max}$) in order to ensure having equal or less voltage ripple than the maximum specified DC-link voltage ripple.

For example, if the DC-link capacitor was designed by means of equation (6.20) and parameters of Table 6.1 , it would result in C_{conv}=398 µF.

Parameter	Value
f_{AC}	50 Hz
ω_o	100·π rad/s
$V_{C,RMS}$	400 V
$\Delta v_{C,pk\text{-}pk}$(%)	5 %
$P_{o,max}$	1000 W
C_{conv}	398 µF

Table 6.1. Parameters for a DC-link capacitor conventional design.

6.3 Design of a reduced DC-link capacitor to supply a constant power load

In this section, the proposed DC-link capacitance reduction is based on the following considerations:

1. The second stage behaves as a constant power load (P_o).
2. The DC-link voltage regulation is carried out by the PFC stage.
3. Load conditions vary very slowly or with limited magnitude of step change.
4. High voltage ripple amplitude is admitted in the DC-link.

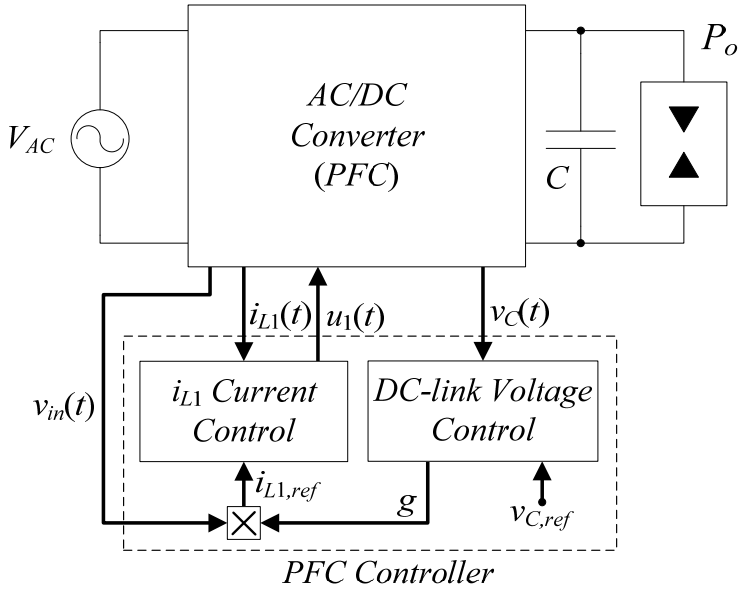


Fig. 6.6. Conventional PFC control design for single-phase applications based on two cascaded stages. Second stage is modelled as a CPL.

Note that points 1 and 2 are commonly used in most of designs (see Fig. 6.6). Point 3 can be assumed in battery charging applications because a battery exhibits very slow load changes.

However, the key point of the proposed DC-link capacitor design for a CPL is given by point 4 which must take into account the second stage's input voltage requirements. Considering that there are no restrictions on the amplitude of the DC-link voltage ripple, the minimum DC-link capacitance value can be calculated so that the DC-link voltage and the rectified input voltage become tangent as illustrated in Fig. 6.7.

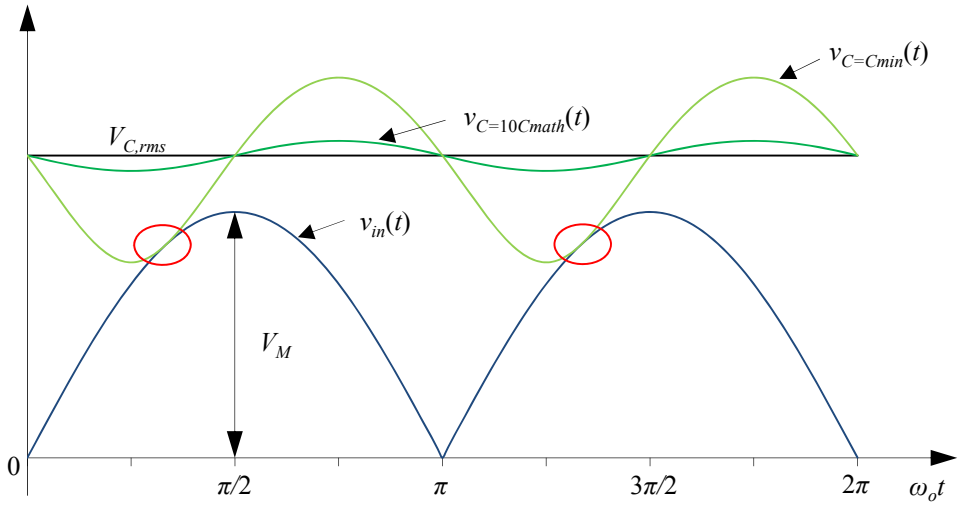


Fig. 6.7. Theoretic DC-link voltage waveforms for C=10C_{math}, C=C_{min} and rectified input voltage $v_{in}(t)$.

6.3.1 Minimum DC-link capacitor design

As commented previously, the minimum DC-link capacitance value corresponds to the capacitance that makes $v_C(t)$ becoming tangent to $v_{in}(t)$ as depicted by voltage $v_{C=Cmin}(t)$ in Fig. 6.7. Hence, the analysis must be started with the following equation $v_{in}(t)=v_{C=Cmin}(t)$.

$$\left|V_M \sin\left(\omega_o t\right)\right| = V_{C,rms}\sqrt{1-\frac{P_o}{C_{\min}\omega_o V_{C,rms}^2}\sin\left(2\omega_o t\right)} \tag{6.21}$$

This resulting in:

$$2\sin\left(\omega_o t\right)\cos\left(\omega_o t\right) = \frac{\omega_o C_{\min}}{P_o}\left(V_{C,rms}^2 - V_M^2\sin^2\left(\omega_o t\right)\right) \tag{6.22}$$

Using the following equalities in (6.22):

$$\begin{aligned}\sin\left(\omega_o t\right) &= \frac{\tan\left(\omega_o t\right)}{\sqrt{1+\tan^2\left(\omega_o t\right)}}\\ \cos\left(\omega_o t\right) &= \frac{1}{\sqrt{1+\tan^2\left(\omega_o t\right)}}\end{aligned} \tag{6.23}$$

It is possible to write:

$$\tan^2\left(\omega_o t\right) + k_1\tan\left(\omega_o t\right) + k_2 = 0 \tag{6.24}$$

Where parameters k_1 and k_2 are defined as

$$k_1 = -\frac{2P_o}{\omega_o C_{\min}\left(V_{C,rms}^2 - V_M^2\right)} \tag{6.25}$$

$$k_2 = \frac{V_{C,rms}^2}{V_{C,rms}^2 - V_M^2} \tag{6.26}$$

It can be deduced from the solution of (6.24) that the following condition has to be fulfilled to force the tangency between $v_C(t)$ and $v_{in}(t)$:

$$\left(k_1\right)^2 - 4k_2 = 0 \tag{6.27}$$

Therefore, the minimum DC-link capacitance is obtained by isolating C_{min} from (6.27):

$$C_{\min} = \frac{P_{o,\max}}{\omega_o V_{C,rms}}\sqrt{\frac{1}{V_{C,rms}^2 - V_M^2}} \tag{6.28}$$

Note again that the minimum DC-link capacitor must be designed according to the maximum power operation of the system ($P_{o,max}$), the required DC-link voltage $V_{C,RMS}$ and the grid characteristics. Moreover, the finally selected capacitor must have a higher capacitance than C_{min} in order to make impossible finding a real solution for equation (6.24) or, in other words, ensuring that in steady-state $v_C(t)$ never meets $v_{in}(t)$, this allowing a proper operation of the boost converter.

In this case, if the DC-link capacitor was designed by means of equation (6.28) and parameters of Table 6.2, it would result in C_{min}=34.18 μF. As it can be seen, the achieved reduction is about eleven times with respect the conventional design. As commented previously, the finally selected capacitance C_{Sel} should be slightly higher than $C_{min,}$. For that reason, a capacitor of 40 μF has been selected for testing purposes.

Parameter	Value
V_M	$230\sqrt{2}$ V
f_{AC}	50 Hz
ω_o	100·π rad/s
$V_{C,RMS}$	400 V
$P_{o,max}$	1000 W
C_{min}	34.18 μF
C_{Sel}	40 μF

Table 6.2. Parameters for the first DC-link capacitance reduction approach.

Fig. 6.8 compares the resulting DC-link capacitance as a function of parameters $P_{o,max}$ and $V_{C,RMS}$ according to the conventional and the proposed design. It is important to remark that this

figure has been obtained considering standard European line characteristics (V_{AC}=230 V_{RMS} and f_{AC}=50 Hz) and $\Delta v_{C,pk\text{-}pk}$(%)=10% for the conventional design. As it can be observed, the necessary DC-link capacitance is clearly reduced by means of the proposed design.

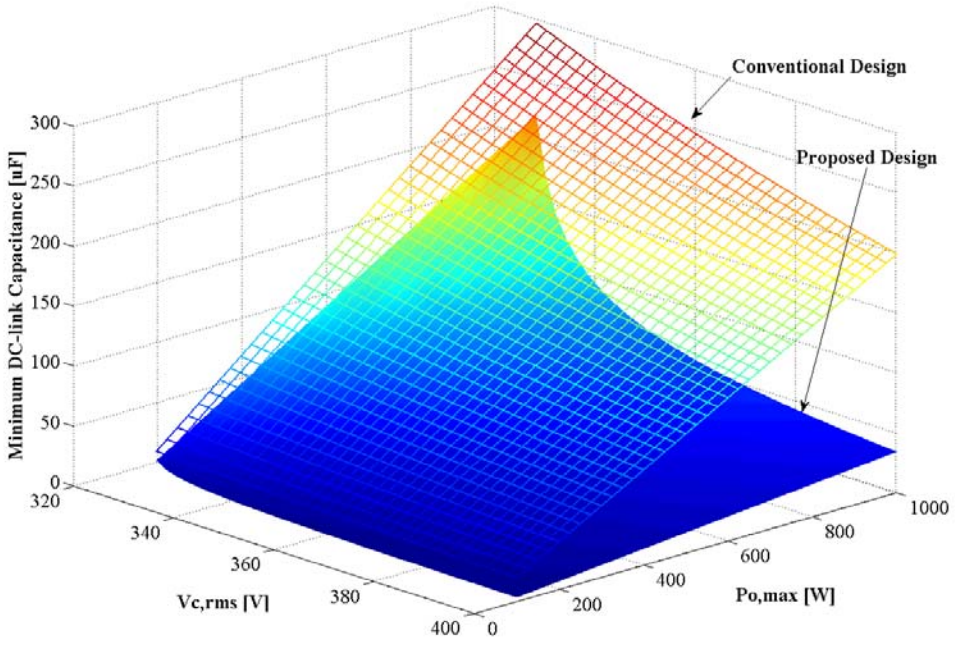


Fig. 6.8. DC-link capacitance according to a conventional design ($\Delta v_{C,pk\text{-}pk}$=10%) and the proposed design as a function of voltage $V_{C,RMS}$ and output power $P_{o,max}$ for V_{AC}=230 V_{RMS} and f_{AC}=50 Hz.

A different way to appreciate the DC-link capacitor reduction is calculating the ratio C_{conv}/C_{min} for the same load and line conditions. It can be demonstrated that this relation results in

$$\frac{C_{conv}}{C_{\min}} = \frac{\sqrt{1-\alpha^2}}{\Delta v_{C,\mathrm{pk-pk}}(\%)} \tag{6.29}$$

where

$$\alpha = \frac{V_M}{V_{C,rms}} \tag{6.30}$$

Note that expression (6.29) only depends on parameters $\Delta v_{C,pk\text{-}pk}$, which is specified on the conventional design, and parameter α, which relates V_M and $V_{C,RMS}$. Therefore, it is possible to plot the resulting reduction depending on these two parameters as in Fig. 6.9. Note that the maximum reduction is given for the minimum $\Delta v_{C,pk\text{-}pk}$(%) and maximum $V_{C,RMS}$ conditions. In this picture it is possible to appreciate that the reduction is about 60 times for $\Delta v_{C,pk\text{-}pk}$(%)=1% and α=0.8125 ($V_M$=325 V and $V_{C,RMS}$=400 V_{RMS}).

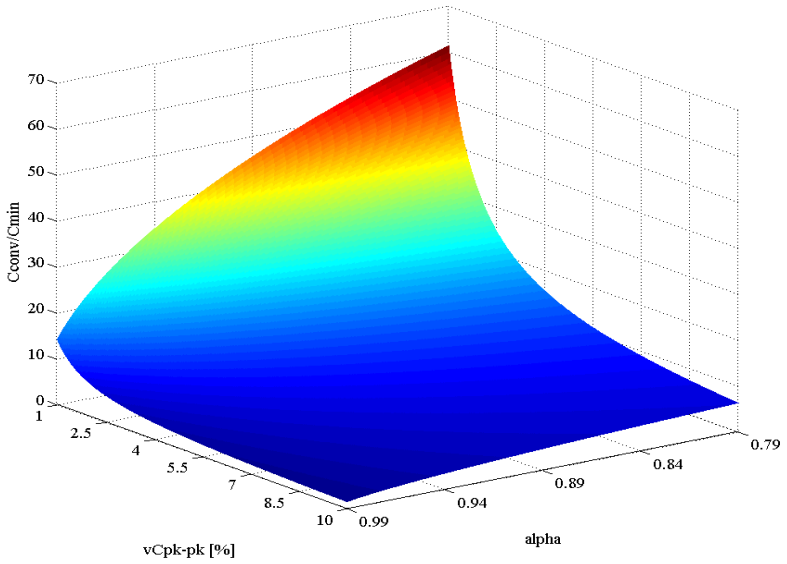


Fig. 6.9. C_{conv}/C_{min} relation depending on $\Delta v_{C,pk\text{-}pk}(\%)$ and α.

Finally, it is worth reminding that voltage ripple of $v_C(t)$ varies with load conditions and that the maximum ripple amplitude is given for full load conditions (see $v_{Cmin,1}(t)$ oscillating at $V_{C,RMS1}$ in Fig. 6.10). However, if the system was operating under lower load conditions, $v_C(t)$ and $v_{in}(t)$ were not tangent anymore if $v_{Cmin,2}(t)$ continued oscillating at $V_{C,RMS1}$. In order to force the tangency between $v_C(t)$ and $v_{in}(t)$ again, the reference of the DC-link voltage controller should be changed to $V_{C,RMS2}$ as illustrated in Fig. 6.10. Note that this adjustment would result in an improvement of the system's efficiency since it did not have to step-up the output voltage as much as before.

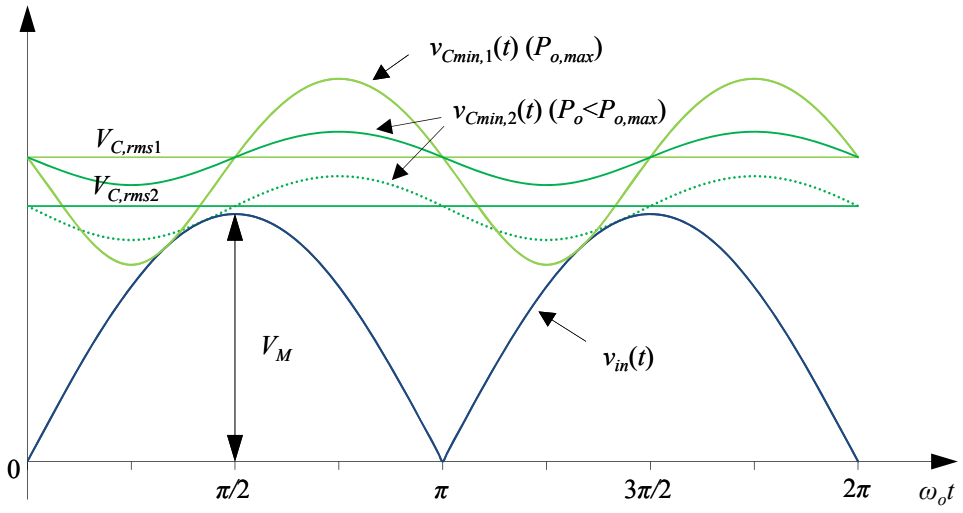


Fig. 6.10. $V_{C,RMS}$ adjustment depending on the load conditions considering the finally selected DC-link capacitance.

The required DC-link voltage reference $V_{C,RMS\text{-}ref}$ can be obtained by solving equation (6.28) for $V_{C,RMS}$ and substitute C_{min} for the finally selected DC-link capacitance C_{Sel}.

$$V_{C,rms-ref} = V_{AC}\sqrt{1+\sqrt{1+\frac{4P_o^{\,2}}{\omega_o^{\,2}C_{Sel}^{\,2}V_M^{\,4}}}} \tag{6.31}$$

The complexity and non-linearity of the previous expression make more recommendable the use of a microcontroller or a field programmable gate array (FPGA) to compute $V_{C,RMS\text{-}ref}$ rather than an analogue circuit.

6.3.2 Constant vs variable switching frequency PFC controllers

Although the proposed DC-link capacitor reduction can yield to a deep discussion about the design of the EMI filter, this study is only focused on PFC controller. It is known that most of PFC controllers operate at a constant switching frequency owing to the advantages regarding the design of filtering stages. However, the high amplitude of the DC-link voltage ripple would generate a high deformation on inductor current ripple $\Delta i_{L1}(t)$ (see Fig. 6.11 and Fig. 6.12.a) if a constant switching frequency controller was employed in this case. As commented in previous chapters, inductor current ripple of a boost converter in CCM operation is defined by the following expression:

$$\Delta i_{L1}(t) = \frac{v_{in}(t)}{F_{SW}L_1}\left(1-\frac{v_{in}(t)}{v_C(t)}\right) \tag{6.32}$$

where F_{SW} is the switching frequency and L_1 is the inductor value of the boost converter. In contrast, hysteretic controllers are not affected by the high voltage oscillations of the DC-link because $\Delta i_{L1}(t)$ is directly determined by the hysteresis width. Hence, $\Delta i_{L1}(t)$ remains constant with value $2H$, where H stands for the positive hysteresis bound (see Fig. 6.11 and Fig. 6.12.b). Furthermore, the performance of hysteretic current-mode controllers can be improved by the two following non-exclusive techniques which consist in modulating the hysteresis width.

a) Hysteresis modulation around the zero-crossing area of the line voltage to improve the zero-crossing distortion [85, 117].
b) Hysteresis modulation depending on the load conditions [118].

The combination of both techniques could be used to obtain an inductor current waveform as the one depicted in Fig. 6.12.c.

Unidirectional converters which are managed by hysteretic current-mode controllers tend to exhibit an important zero-crossing distortion in PFC applications due to the high decrease of the switching frequency in this area. In the particular case of boost converters, or boost-derived structures, the system stops switching when inductor current reaches 0 A (see Fig. 6.13.a) and remains switched off until the difference between inductor current and its reference is capable to reach one hysteresis bound again.

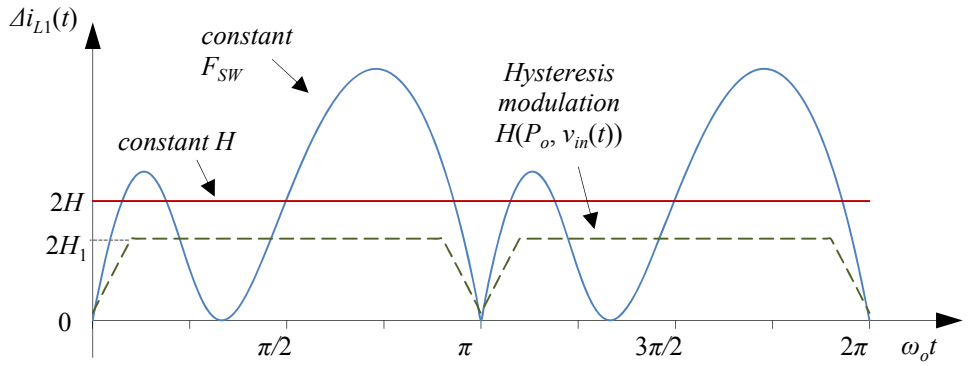


Fig. 6.11. Inductor current ripple depending on the applied control technique: constant switching frequency-based controller, hysteretic current-mode controller with constant hysteresis or modulated hysteresis.

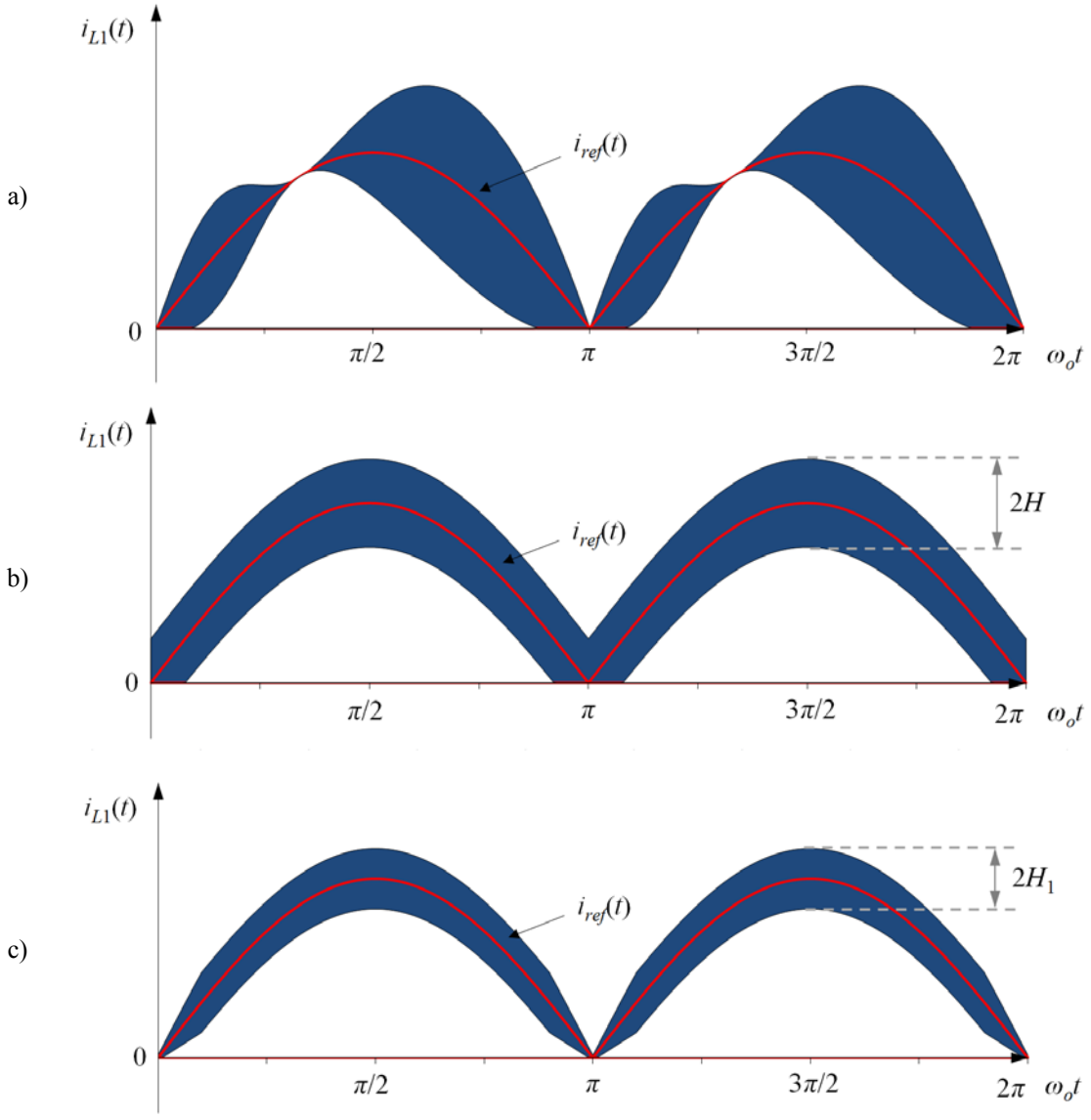


Fig. 6.12. Theoretic inductor current under different current-mode control techniques. a) Constant switching frequency-based controller. b) Constant hysteresis-based controller. c) Modulated hysteresis-based controller.

One solution to ensure the switching operation around the zero-crossing area is to reduce the hysteresis bounds as depicted in Fig. 6.13.b. This approach results in a lower THD with the expense of increasing the switching frequency [117]. Experimental results depicted in Fig. 6.13 have been obtained from a semi-bridgeless boost converter with a hysteretic current-mode controller [82].

On the other hand, hysteresis modulation depending on load conditions [118] allows achieving a lower THD because inductor current ripple is reduced with load conditions and, in consequence, the ratio current ripple / average current is also reduced.

a)

b)

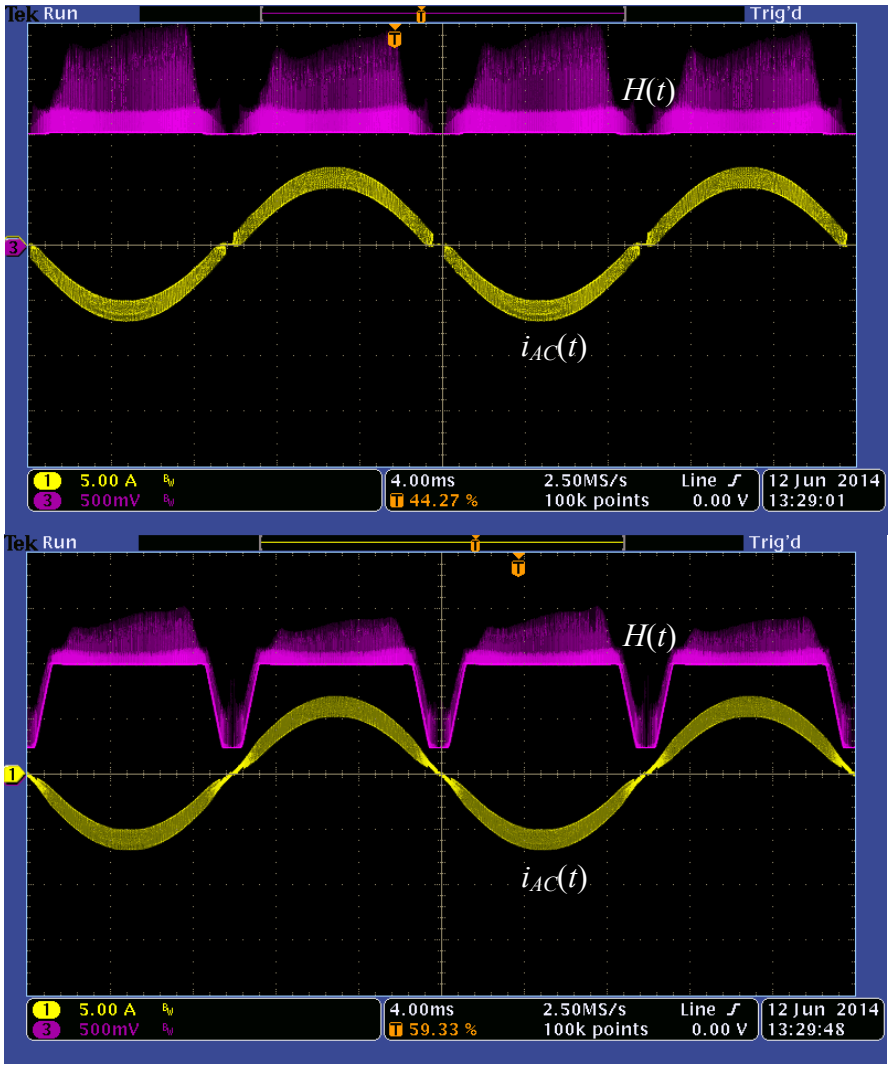


Fig. 6.13. Line current under hysteretic current-mode control with a) constant hysteresis, b) modulated hysteresis. CH1: line current $i_{AC}(t)$ (5 A/div), CH3: hysteresis signal $H(t)$ (500 mV/div).

Thus, it makes sense supposing that hysteretic current controllers can lead to better PF and THD with respect fixed-frequency-based PFC current-mode controllers due to their intrinsic capability to keep the width of inductor current ripple limited. For that reason, the inner control loop of the here employed PFC controller consists of a hysteretic current-mode controller with

hysteresis modulation (see Fig. 6.14). As it can be observed, signal $H(t)$ will be only modulated depending on the rectified input voltage to reduce the zero-crossing distortion similarly to Fig. 6.13.b. Inductor current reference is given by the multiplication of $v_{in}(t)$ and conductance $g(t)$, which comes from a conventional PI controller that regulates voltage $v_C(t)$.

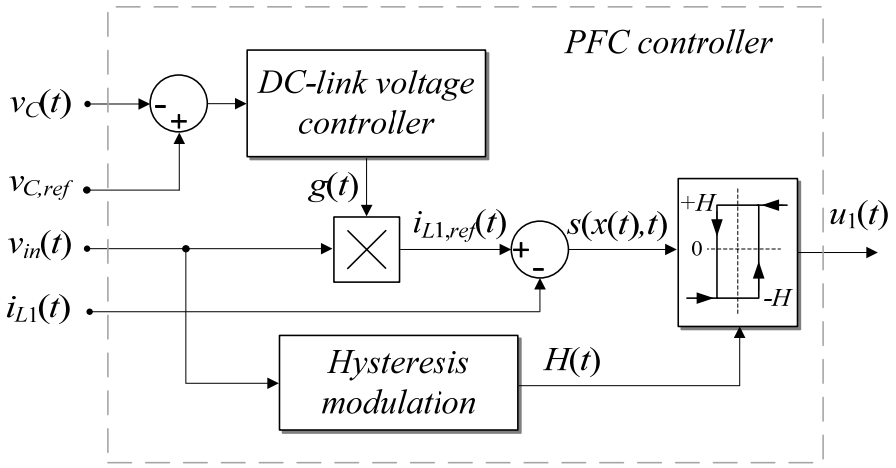


Fig. 6.14. Block diagram of the proposed PFC controller.

6.3.3 Sliding-mode control application

Continuous-time sliding-mode control [76] is employed to describe the dynamic behaviour of the switching converter since a hysteretic current-mode controller is employed.

Similarly to previous chapters, the analysis starts with the plant modelling. In order to simplify the analysis, the boost converter is considered an ideal system that operates in CCM. If the state vector of the power stage is defined as

$$x(t)=\begin{bmatrix} i_{L1}(t) \\ v_C(t) \end{bmatrix} \tag{6.33}$$

the dynamics of the boost converter can be expressed by means of the following differential equations.

$$\dot{x}(t)=A_1x(t)+B_1, \quad for\ u_1(t)=1 \tag{6.34}$$

$$\dot{x}(t)=A_2x(t)+B_2, \quad for\ u_1(t)=0 \tag{6.35}$$

Symbol ˙ represents the time derivative function and $u_1(t)$ is the control signal that determines the state of the MOSFET. Matrices A_1, A_2, B_1 and B_2 are defined as follows according to the conduction topologies of a boost converter that are depicted in Fig. 6.15.

$$A_1=\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad A_2=\begin{bmatrix} 0 & -\frac{1}{L_1} \\ \frac{1}{C_{Sel}} & 0 \end{bmatrix}, \quad B_1=B_2=\begin{bmatrix} \frac{v_{in}(t)}{L_1} \\ \frac{-i_o(t)}{C_{Sel}} \end{bmatrix} \tag{6.36}$$

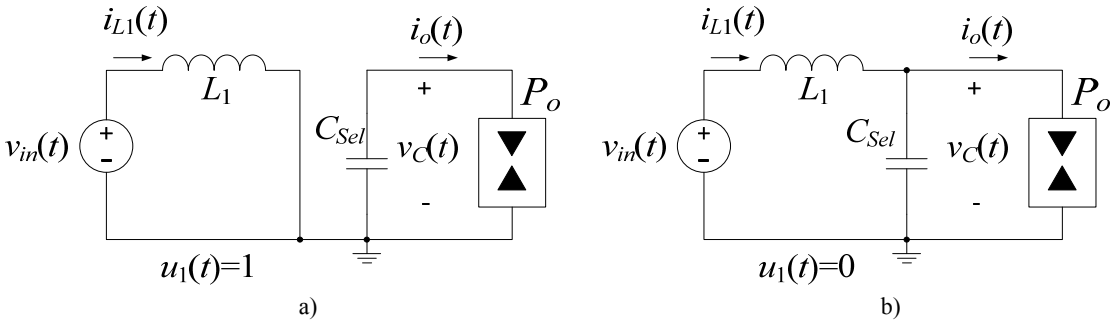


Fig. 6.15. Conduction topologies of a boost converter. a) ON-state. b) OFF-state.

Differential equations (6.34) and (6.35) can be combined in only one bilinear expression:

$$\dot{x}(t) = A_2 x(t) + B_2 + \left[(A_1 - A_2) x(t) + (B_1 - B_2) \right] u_1(t) \tag{6.37}$$

To impose an LFR behaviour on the PFC stage [78], sliding control surface $s(x(t),t)$ must be chosen as :

$$s(x(t),t) = i_{L1}(t) - g(t) \cdot v_{in}(t) \tag{6.38}$$

which in sliding-mode regime becomes $s(x(t),t)=0$ and, in consequence, inductor current is proportional to the rectified input voltage. Variable $g(t)$ stands for the conductance of the PFC stage and it is generated by the PI controller that regulates $v_C(t)$. Sliding control surface can be defined as a function of $x(t)$ as follows:

$$s(x(t),t) = Kx(t) - i_{L1,ref}(t) \tag{6.39}$$

where

$$K = [1 \;\; 0] \tag{6.40}$$

$$i_{L1,ref}(t) = g(t) v_{in}(t) \tag{6.41}$$

The discontinuous control action $u(t)$ depends on the sign of the switching function as follows in order to induce a sliding-mode regime.

$$u_1(t) = \begin{cases} 0 & if \quad s(x,t) > 0 \\ 1 & if \quad s(x,t) < 0 \end{cases} \tag{6.42}$$

To reach the sliding-mode surface it is necessary to fulfil the reachability conditions, which can be obtained from the following condition

$$s(x(t),t) \cdot \frac{\mathrm{d}s(x(t),t)}{\mathrm{d}t} < 0 \tag{6.43}$$

The time derivate of switching function $s(x(t),t)$ defined in (6.39) is

$$\begin{aligned}\frac{\mathrm{d}s\left(x(t),t\right)}{\mathrm{d}t} &= K\dot{x}(t) - \frac{\mathrm{d}\left(i_{L1,ref}(t)\right)}{\mathrm{d}t} = \\ &= K\left(A_2x(t)+B_2+\left[\left(A_1-A_2\right)x(t)+\left(B_1-B_2\right)\right]u_1(t)\right) - \frac{\mathrm{d}\left(i_{L,ref}(t)\right)}{\mathrm{d}t}\end{aligned} \tag{6.44}$$

Hence, it is possible to demonstrate that the reachability conditions for a boost converter are the following

$$v_C(t) > v_{in}(t) \quad if \quad s\left(x(t),t\right) > 0 \tag{6.45}$$

$$v_{in}(t) > 0 \quad if \quad s\left(x(t),t\right) < 0 \tag{6.46}$$

Note that (6.45) is satisfied in a boost converter under steady-state operation and (6.46) is also fulfilled since $v_{in}(t)$ represents the rectified input voltage.

According to the equivalent control method [76], a necessary condition for the existence of a sliding motion on the switching surface is the given by the transversality or existence condition, which is

$$\frac{\partial}{\partial u_1(t)}\left(\frac{\mathrm{d}s\left(x(t),t\right)}{\mathrm{d}t}\right) = K\left[\left(A_1-A_2\right)x(t)+\left(B_1-B_2\right)\right] \neq 0 \tag{6.47}$$

In the particular case of a boost converter, transversality condition (6.47) is fulfilled as long as

$$v_C(t) \neq 0 \tag{6.48}$$

which is accomplished since $v_C(t)>0$. Then, imposing

$$\left.\frac{\mathrm{d}s\left(x(t),t\right)}{\mathrm{d}t}\right|_{u_1(t)=u_{1,eq}(t)} = 0 \tag{6.49}$$

on (6.44) leads to the equivalent control expression

$$u_{1,eq}(t) = \frac{\dfrac{\mathrm{d}\left(i_{L1,ref}(t)\right)}{\mathrm{d}t} - K\left(A_2x(t)+B_2\right)}{K\left[\left(A_1-A_2\right)x(t)+\left(B_1-B_2\right)\right]} \tag{6.50}$$

Equivalent control $u_{1,eq}(t)$ is defined as the smooth control law that ideally constrains the state trajectories on the switching surface once reached. Then, sliding-mode exists satisfying

$$0 < u_{1,eq}(t) < 1\,, \tag{6.51}$$

if (6.47) is positive. In this sense, equivalent control $u_{1,eq}(t)$ of a boost converter is

$$u_{1,eq}(t) = \frac{L_1\dfrac{\mathrm{d}\left(i_{L1,ref}(t)\right)}{\mathrm{d}t} + v_C(t) - v_{in}(t)}{v_C(t)} \tag{6.52}$$

The ideal sliding-mode dynamics [119] can be obtained by considering that the system is in sliding-mode regime $s(x(t),t)=0$ and substituting $u_1(t)$ for $u_{1,eq}(t)$ in (6.37).

$$\dot{i}_{L1}(t)=\frac{\mathrm{d}\left(i_{L1,ref}(t)\right)}{\mathrm{d}t} \tag{6.53}$$

$$\dot{v}_C(t)=-\left(\frac{L_1 g(t) v_{in}(t)}{C_{Sel} v_C(t)}\right)\frac{\mathrm{d}\left(i_{L1,ref}(t)\right)}{\mathrm{d}t}+\frac{g(t)\left(v_{in}(t)\right)^2}{C_{Sel} v_C(t)}-\frac{i_o(t)}{C_{Sel}} \tag{6.54}$$

As it can be observed, the inductor current dynamics exhibits the inductor current reference dynamics. Finally, it is important to remark that

$$\frac{\mathrm{d}\left(i_{L1,ref}(t)\right)}{\mathrm{d}t}=\dot{g}(t) v_{in}(t)+g(t)\dot{v}_{in}(t) \tag{6.55}$$

6.3.4 Small-signal modelling

Similarly to previous chapters, it is necessary to derive conductance to DC-link voltage transfer function $G_{GVc}(s)$ before designing the DC-link voltage controller $G_1(s)$. Linearizing (6.54) around the equilibrium point (X^*) results

$$\begin{aligned}\dot{\tilde{v}}_C(t)\simeq&\left.\frac{\partial \dot{v}_C(t)}{\partial v_C(t)}\right|_{X^*}\tilde{v}_C(t)+\left.\frac{\partial \dot{v}_C(t)}{\partial \dot{g}(t)}\right|_{X^*}\dot{\tilde{g}}(t)+\left.\frac{\partial \dot{v}_C(t)}{\partial g(t)}\right|_{X^*}\tilde{g}(t)+\left.\frac{\partial \dot{v}_C(t)}{\partial \dot{v}_{in}(t)}\right|_{X^*}\dot{\tilde{v}}_{in}(t)+\\&+\left.\frac{\partial \dot{v}_C(t)}{\partial v_{in}(t)}\right|_{X^*}\tilde{v}_{in}(t)+\left.\frac{\partial \dot{v}_C(t)}{\partial i_o(t)}\right|_{X^*}\tilde{i}_o(t)\end{aligned} \tag{6.56}$$

where

$$\left.\frac{\partial \dot{v}_C(t)}{\partial v_C(t)}\right|_{X^*}=-\frac{g\left(V_{AC}\right)^2}{C_{Sel}\left(V_C\right)^2} \tag{6.57}$$

$$\left.\frac{\partial \dot{v}_C(t)}{\partial \dot{g}(t)}\right|_{X^*}=-\frac{g\left(V_{AC}\right)^2 L_1}{C_{Sel} V_C} \tag{6.58}$$

$$\left.\frac{\partial \dot{v}_C(t)}{\partial g(t)}\right|_{X^*}=\frac{\left(V_{AC}\right)^2}{C_{Sel} V_C} \tag{6.59}$$

$$\left.\frac{\partial \dot{v}_C(t)}{\partial \dot{v}_{in}(t)}\right|_{X^*}=-\frac{g^2 V_{AC} L_1}{C_{Sel} V_C} \tag{6.60}$$

$$\left.\frac{\partial \dot{v}_C(t)}{\partial v_{in}(t)}\right|_{X^*}=\frac{2gV_{AC}}{C_{Sel} V_C} \tag{6.61}$$

$$\left.\frac{\partial \dot{v}_C(t)}{\partial i_o(t)}\right|_{X^*}=-\frac{1}{C_{Sel}} \tag{6.62}$$

Therefore, it is possible to represent the small-signal dynamics of $v_C(t)$ as a function of the corresponding reference, input and perturbation signals as depicted by Fig. 6.16. Transfer functions $Z_o(s)$, $G_{VinVc}(s)$ and $G_{GVc}(s)$ are derived afterwards. Finally, the proposed PI voltage controller for $G_1(s)$ has the following form:

$$G_1(s) = k_p \frac{(k_i s + 1)}{s} \tag{6.63}$$

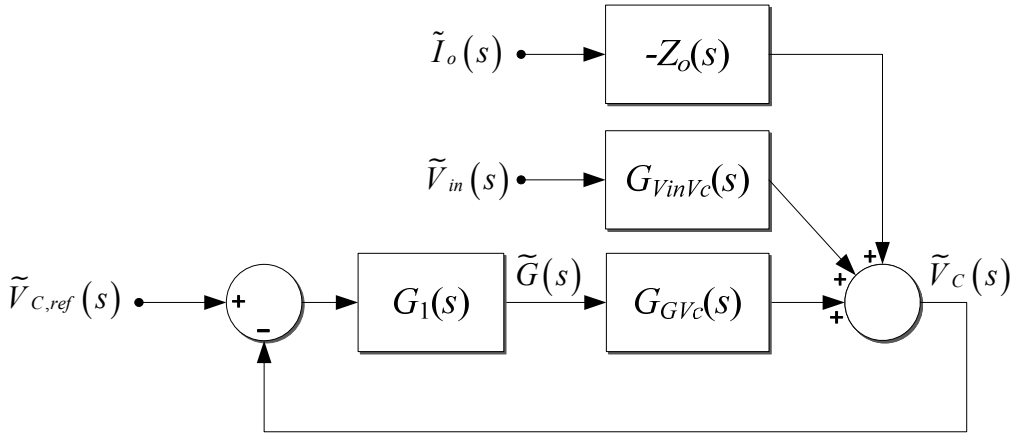


Fig. 6.16. Small-signal representation of the PFC stage.

6.3.4.1 Conductance to DC-link voltage transfer function

Conductance to DC-link voltage transfer function $G_{GVc}(s)$ is obtained by imposing $\dot{\tilde{v}}_{in}(t) = 0$, $\tilde{v}_{in}(t) = 0$ and $\tilde{i}_o(t) = 0$ on (6.56), and applying a Laplace transformation afterwards on the result.

$$G_{GVc}(s) = \frac{\tilde{V}_C(s)}{\tilde{G}(s)} = -\left(\frac{(V_{AC})^2 gL_1}{C_{Sel} V_C}\right) \frac{\left(s - \frac{1}{gL_1}\right)}{\left(s + \frac{g(V_{AC})^2}{C_{Sel}(V_C)^2}\right)} \tag{6.64}$$

The previous expression can be approximated by the following one because the effect of the high-frequency non-minimum phase zero can be neglected for low-frequency conditions.

$$G_{GVc}(s) = \frac{\tilde{V}_C(s)}{\tilde{G}(s)} = \left(\frac{(V_{AC})^2}{C_{Sel} V_C}\right) \frac{1}{\left(s + \frac{g(V_{AC})^2}{C_{Sel}(V_C)^2}\right)} \tag{6.65}$$

6.3.4.2 Open-loop output impedance transfer function

Open-loop output impedance transfer function $Z_o(s)$ is obtained by imposing $\dot{\widetilde{v}}_{in}(t)=0$, $\widetilde{v}_{in}(t)=0$, $\dot{\tilde{g}}(t)=0$ and $\tilde{g}(t)=0$ on (6.56), and applying a Laplace transformation afterwards on the result.

$$Z_o(s)=-\frac{\tilde{V}_C(s)}{\tilde{I}_o(s)}=\frac{1}{C_{Sel}\left(s+\dfrac{g\left(V_{AC}\right)^2}{C_{Sel}\left(V_C\right)^2}\right)} \tag{6.66}$$

Note that the negative sign in (6.66) is due to the definition of $i_o(t)$ going from the 1st stage to the 2nd one (see Fig. 6.17), whereas $Z_o(s)$ represents the impedance in the frequency domain that the 1st stage exhibits towards to its output port.

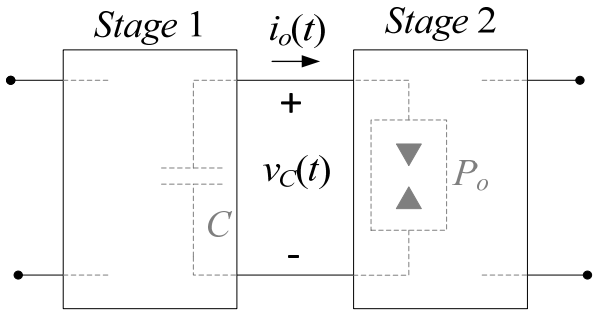


Fig. 6.17. System model based on two cascaded stages.

6.3.4.3 Input voltage to output voltage transfer function

Although input voltage to output voltage transfer function $G_{VinVc}(s)$ is not employed in this work, it can be obtained by imposing $\dot{\tilde{g}}(t)=0$, $\tilde{g}(t)=0$ and $\tilde{i}_o(t)=0$ on (6.56), and applying a Laplace transformation next on the result.

$$G_{VinVc}(s)=\frac{\tilde{V}_C(s)}{\tilde{V}_{in}(s)}=-\left(\frac{g^2V_{AC}L_1}{C_{Sel}V_C}\right)\frac{\left(s-\dfrac{2}{gL_1}\right)}{\left(s+\dfrac{g\left(V_{AC}\right)^2}{C_{Sel}\left(V_C\right)^2}\right)} \tag{6.67}$$

Also, the following transfer function can be a valid approximation of (6.67) for low frequency conditions.

$$G_{VinVc}(s)=\frac{\tilde{V}_C(s)}{\tilde{V}_{in}(s)}=\left(\frac{gV_{AC}}{C_{Sel}V_C}\right)\frac{1}{\left(s+\dfrac{g\left(V_{AC}\right)^2}{C_{Sel}\left(V_C\right)^2}\right)} \tag{6.68}$$

6.3.5 DC-link voltage controller design based on Middlebrook's stability criterion

Special care has to be taken when designing the DC-link voltage controller in this case due to the high reduction of the intermediate capacitor. Traditional method consists in calculating the characteristic equation of the system loop gain $T(s)=G_1(s)G_{GVc}(s)$ to determine the stability limits. Then, controller parameters are adjusted using classical Bode or pole assignment techniques [120]. However, in this work a different strategy is proposed. It consists in an impedance-oriented design that fulfils Middlebrook's stability criterion [121]. The advantage of the proposed design is that it allows a straight forward and stable design of the DC-link voltage controller depending on the components of the plant and the desired cut-off frequency ω_C of $T(s)$. Middlebrook's stability criterion states that the magnitude of the closed-loop output impedance exhibited by the first stage has to be lower than the input impedance of the second stage (see Fig. 6.17).

$$\left|Z_{o-CL,1^{st}}(s)\right| < \left|Z_{in,2^{nd}}(s)\right| \tag{6.69}$$

On one hand, closed-loop output impedance of the first stage $Z_{o\text{-}CL,1^{st}}(s)$ around the equilibrium point is given by the following expression:

$$Z_{o-CL,1^{st}}(s) = \frac{Z_o(s)}{1+T(s)} \tag{6.70}$$

where $Z_o(s)$ is the open-loop output impedance of the first stage defined in (6.66) while $T(s)$ is the loop gain of the system.

$$T(s) = G_1(s)G_{GVc}(s) \tag{6.71}$$

On the other hand, the input impedance of the second stage is given by the negative impedance exhibited by the CPL as depicted in Fig. 6.17.

$$Z_{in,2^{nd}}(s) = -\frac{{V_C}^2}{P_o} \tag{6.72}$$

Substituting (6.63), (6.65) and (6.66) in (6.70), it can be demonstrated that the closed-loop output impedance is given by the following expression:

$$Z_{o-CL,1^{st}}(s) = \frac{1}{C_{Sel}}\left(\frac{s}{s^2+\left(\frac{{V_{AC}}^2}{C_{Sel}\left(V_C\right)^2}\right)\left(g+k_p k_i V_C\right)s+\frac{k_p\left(V_{AC}\right)^2}{C_{Sel}V_C}}\right) \tag{6.73}$$

It is also possible to demonstrate that the maximum magnitude of (6.73) is given when its phase is 0º, this implying that the phase of the numerator and the denominator have to be equal.

$$Z_{o-CL,1^{st}}(j\omega)=\frac{1}{C_{Sel}}\left(\frac{j\omega}{-\omega^2+\left(\frac{{V_{AC}}^2}{C_{Sel}\left(V_C\right)^2}\right)\left(g+k_pk_iV_C\right)(j\omega)+\frac{k_p\left(V_{AC}\right)^2}{C_{Sel}V_C}}\right) \tag{6.74}$$

As it can be observed, the phase of the numerator is 90º. Therefore, the real part of the denominator must be equal to 0:

$$-{\omega_{\max}}^2+\frac{k_p\left(V_{AC}\right)^2}{C_{Sel}V_C}=0 \tag{6.75}$$

where ω_{max} stands for the angular frequency at which the closed-loop output impedance (6.73) reaches its maximum magnitude. Thus, solving (6.75) for ω_{max} results in

$$\omega_{\max}=V_{AC}\sqrt{\frac{k_p}{C_{Sel}V_C}} \tag{6.76}$$

Hence, the maximum magnitude of the closed-loop output impedance in dBs is given by the following expression.

$$\left|Z_{o-CL,1^{st}}(j\omega_{\max})\right|=20\log\left(\frac{{V_C}^2}{\left({V_{AC}}^2\right)\left(g+k_pk_iV_C\right)}\right) \tag{6.77}$$

Therefore, if the input impedance of the second stage is assumed to be constant and Middlebrook's stability criterion is satisfied for the maximum magnitude of the closed-loop output impedance, the stability of the system will be automatically satisfied for the rest of low-frequency spectrum.

$$\left|Z_{o-CL,1^{st}}(j\omega_{\max})\right|<\left|Z_{in,2^{nd}}(j\omega)\right| \tag{6.78}$$

The previous expression becomes:

$$\frac{{V_C}^2}{\left({V_{AC}}^2\right)\left(g+k_pk_iV_C\right)}<\frac{{V_C}^2}{P_o} \tag{6.79}$$

which can be rewritten as follows.

$$P_o<\left({V_{AC}}^2\right)\left(g+k_pk_iV_C\right) \tag{6.80}$$

Assuming that the difference in dBs between the input impedance of the second stage and the maximum closed-loop output impedance of the first stage is sufficiently low according to designer's criteria, it is possible to define the impedance difference as follows.

$$\Delta Z_{dif}=\left|Z_{in,2^{nd}}(j\omega)\right|-\left|Z_{o-CL,1^{st}}(j\omega_{\max})\right| \tag{6.81}$$

It is possible to use ΔZ_{dif} to define the following parameter

$$k_{dif} = 10^{\frac{\Delta Z_{dif}}{20}} \tag{6.82}$$

Note that k_{dif} will be always higher than 1 since ΔZ_{dif} has to be always positive. Besides, it will be seen afterwards that there exists a maximum value for k_{dif}. The previous parameter is used in the left hand side of inequality (6.80) in order to write the following expression.

$$k_{dif} P_o = \left(V_{AC}{}^2\right)\left(g + k_p k_i V_C\right) \tag{6.83}$$

Considering that in the equilibrium point $gV_{AC}{}^2=P_{in}$ and $P_o=P_{in}$, expression (6.83) results in the following expression.

$$\left(k_{dif} - 1\right) P_o = k_p k_i V_C \left(V_{AC}\right)^2 \tag{6.84}$$

Therefore, parameter k_p of the PI controller can be set as follows.

$$k_p = \frac{\left(k_{dif} - 1\right) P_o}{k_i V_C \left(V_{AC}\right)^2} \tag{6.85}$$

On the other hand, the definition of parameter k_i is obtained from the desired cut-off angular frequency ω_C of loop gain $T(s)$. If $G_{GVc}(s)$ is redefined in a general form as follows:

$$G_{GVc}\left(s\right) = \frac{\tilde{V}_C\left(s\right)}{\tilde{G}\left(s\right)} = k_1 \frac{1}{\left(s + p_1\right)} \tag{6.86}$$

where k_1 and p_1 are defined by (6.65) as:

$$k_1 = \frac{V_{AC}{}^2}{C_{Sel} V_C} \tag{6.87}$$

$$p_1 = \frac{g\left(V_{AC}\right)^2}{C_{Sel}\left(V_C\right)^2} \tag{6.88}$$

it is possible to find one expression for ω_C and k_i respectively. Firstly, loop gain $T(s)$ is defined as:

$$T\left(s\right) = G_1\left(s\right) G_{GVc}\left(s\right) = k_p \frac{\left(k_i s + 1\right)}{s} k_1 \frac{1}{\left(s + p_1\right)} \tag{6.89}$$

so that magnitude of $T(s)$ in dBs is defined as follows.

$$\left|T\left(j\omega\right)\right| = 20 \cdot \log\left(\frac{k_1 k_p \sqrt{\left(k_i \omega\right)^2 + 1}}{\omega \sqrt{\omega^2 + p_1{}^2}}\right) \tag{6.90}$$

Knowing that $|T(j\omega_C)|=0$ dB, it possible to derive the following equation.

$$\frac{k_1 k_p \sqrt{\left(k_i \omega_C\right)^2 + 1}}{\omega_C \sqrt{\omega_C{}^2 + p_1{}^2}} = 1 \tag{6.91}$$

Solving equation (6.91) for ω_C results in the following expression:

$$\omega_C = \sqrt{\frac{\sqrt{\left(p_1{}^2 - \left(k_p k_i k_1\right)^2\right)^2 + 4\left(k_p k_1\right)^2} - \left(p_1{}^2 - \left(k_p k_i k_1\right)^2\right)}{2}} \tag{6.92}$$

while k_i is given by the following one.

$$k_i = \frac{\sqrt{\left(\omega_C p_1\right)^2 + \omega_C{}^4 - \left(k_p k_1\right)^2}}{\omega_C k_p k_1} \tag{6.93}$$

Considering that k_p is defined by (6.85) and $P_{in}=V_{AC}{}^2 \cdot g = P_o$, k_i results in

$$k_i = \frac{\left(k_{dif} - 1\right) P_o}{\omega_C \sqrt{\left(C_{Sel} \omega_C \left(V_C\right)^2\right)^2 + k_{dif}\left(2 - k_{dif}\right)\left(P_o\right)^2}} \tag{6.94}$$

As commented previously, k_{dif} presents an upper limit, this implying that ΔZ_{dif} is also upper limited and its maximum value depends on the system parameters. The maximum value of k_{dif} can be found by solving the denominator of expression (6.94) for zero value, i.e.

$$k_{dif,\max} = 1 + \sqrt{1 + \left(\frac{C_{Sel} \omega_C \left(V_C\right)^2}{P_o}\right)^2} \tag{6.95}$$

Hence, k_{dif} is limited as follows

$$1 < k_{dif} < 1 + \sqrt{1 + \left(\frac{C_{Sel} \omega_C \left(V_C\right)^2}{P_o}\right)^2} \tag{6.96}$$

Table 6.3 collects power stage parameters that are necessary to design the DC-link voltage controller.

Parameter	Value
V_{AC}	230 V_{RMS}
V_C	400 V
C_{Sel}	40 µF
P_o	1000 W
g	18.9 mS

Table 6.3. Power stage parameter values.

Hence, for a DC-link voltage controller design with a fixed cut-off frequency f_C, it is possible to find a maximum value for k_{dif} and ΔZ_{dif}. It is important adjusting f_C sufficiently below twice the line frequency harmonic to avoid an important line current distortion. If for example, f_C was selected as 10 Hz, k_{dif} and ΔZ_{dif} are limited as follows according to parameters listed in Table 6.3.

$$1 < k_{dif} < 2.0778 \tag{6.97}$$

$$0 < \Delta Z_{dif} < 6.3521 \text{ dB} \tag{6.98}$$

Three different values of ΔZ_{dif} have been considered to compare the resulting frequency response of both loop gain and closed-loop output impedance. Parameters ΔZ_{dif}, k_{dif}, k_i and k_p of each design are specified in Table 6.4.

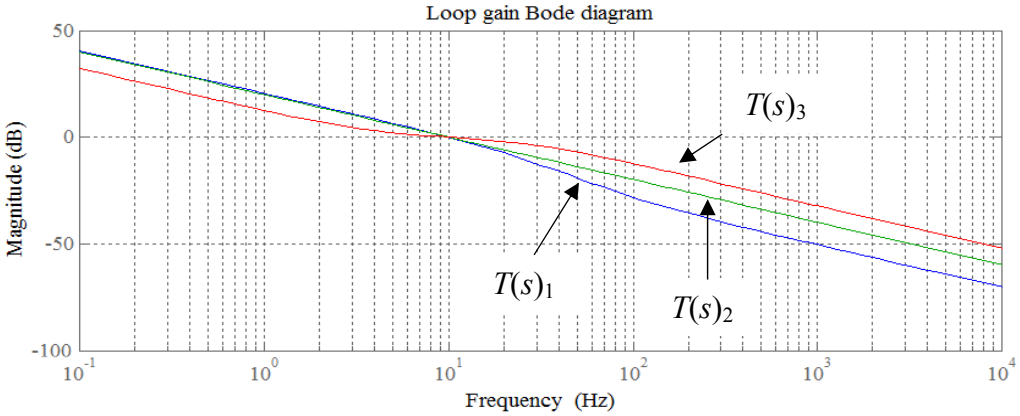
ΔZ_{dif} [dB]	k_{dif}	k_i	k_p	$T(s)$	$Z_{o\text{-}CL,1st}(s)$
1	1.1220	$1.8 \cdot 10^{-3}$	$3.2 \cdot 10^{-3}$	$T(s)_1$	$Z_{o\text{-}CL}(s)_1$
3	1.4125	$6.6 \cdot 10^{-3}$	$3 \cdot 10^{-3}$	$T(s)_2$	$Z_{o\text{-}CL}(s)_2$
6	1.9953	$38.3 \cdot 10^{-3}$	$1.2 \cdot 10^{-3}$	$T(s)_3$	$Z_{o\text{-}CL}(s)_3$

Table 6.4. Design of three different DC-link voltage controllers with the same cut-off frequency.

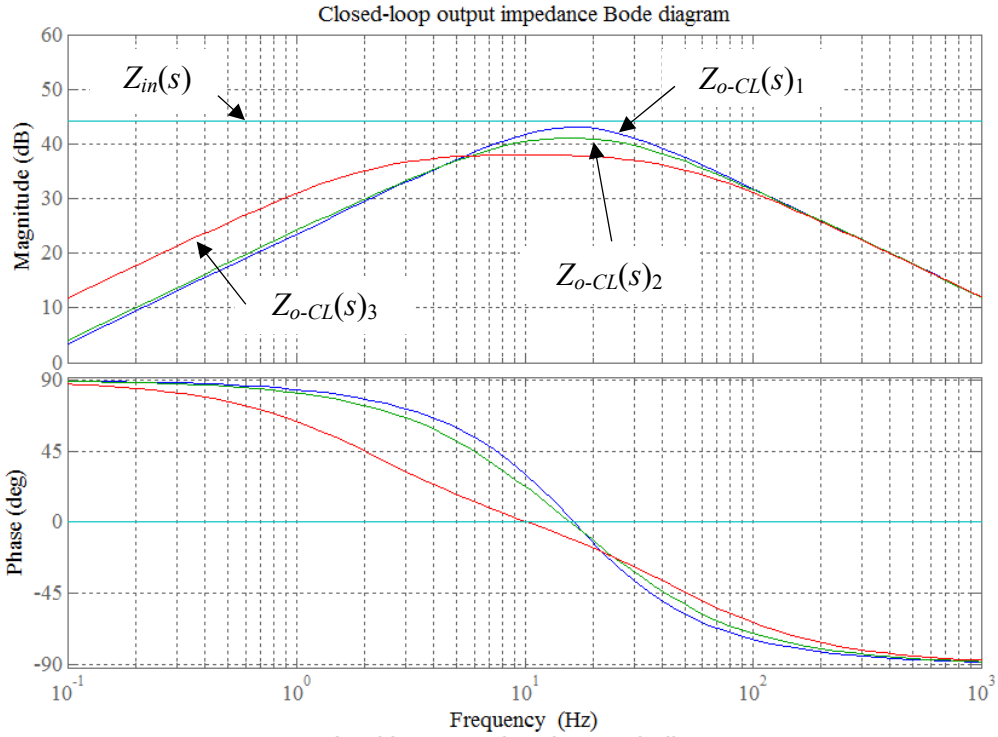
The resulting frequency response for each controller is illustrated in Fig. 6.18. It is possible to observe in Fig. 6.18.a that the loop gain magnitude of all controllers crosses the level of 0 dB at 10 Hz as desired. Furthermore, Fig. 6.18.b confirms that magnitude of any $Z_{o\text{-}CL,1}^{st}(s)$ is lower than $Z_{in}(s)$ and Fig. 6.18.c depicts a closer view around the maximum magnitude of the three different $Z_{o\text{-}CL,1}^{st}(s)$. Note that the lowest attenuation of the loop gain magnitude above the cut-off frequency corresponds to the highest value of ΔZ_{dif}. Thus, input current distortion at twice the line frequency would be higher for high values of ΔZ_{dif}. In contrast, a higher attenuation of the loop gain above the cut-off frequency implies decreasing the value of ΔZ_{dif}, which is not recommended either. Hence, the appropriate selection of ΔZ_{dif} consists in a trade-off between having enough impedance difference and magnitude attenuation above the cut-off frequency. For that reason, ΔZ_{dif}=3 dB has been selected as the most suitable value.

It is also possible to compare the resulting frequency response in case of designing three controllers with the same ΔZ_{dif}= 3 dB (k_{dif}=1.4125) but different cut-off frequency. Table 6.5 collects control design parameters for three different cut-off frequencies: 1 Hz, 4 Hz and 10 Hz. Fig. 6.19.a depicts how the loop gain magnitude of each controller crosses 0 dB at the specified cut-off frequency and Fig. 6.19.b shows that $Z_{in}(s)$ is always higher than $Z_{o\text{-}CL,1}^{st}(s)$. Note that the frequency interval for which impedances difference is minimum increases with the decrease of the cut-off frequency. Therefore, selecting a very low value for the cut-off frequency is not either recommended, so that f_C=10 Hz is suitable enough.

a)



b)



c)

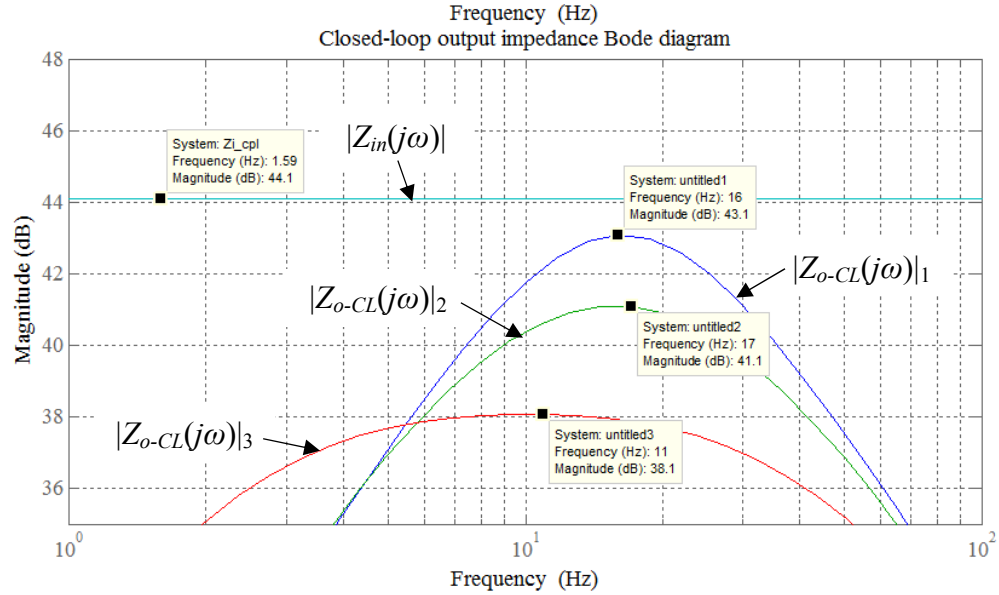
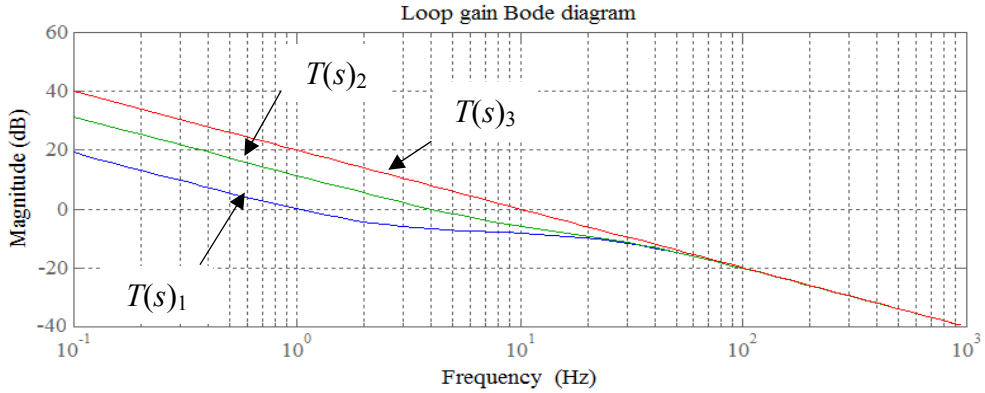


Fig. 6.18. Bode diagram of a) loop gain, b) closed-loop output impedance $Z_{o\text{-}CL,1st}(s)$ and $Z_{in}(s)$, c) detail of the maximum magnitudes. Sub-indexes 1, 2 and 3 stands for ΔZ_{dif} 1 dB, 3 dB and 6 dB designs.

a)



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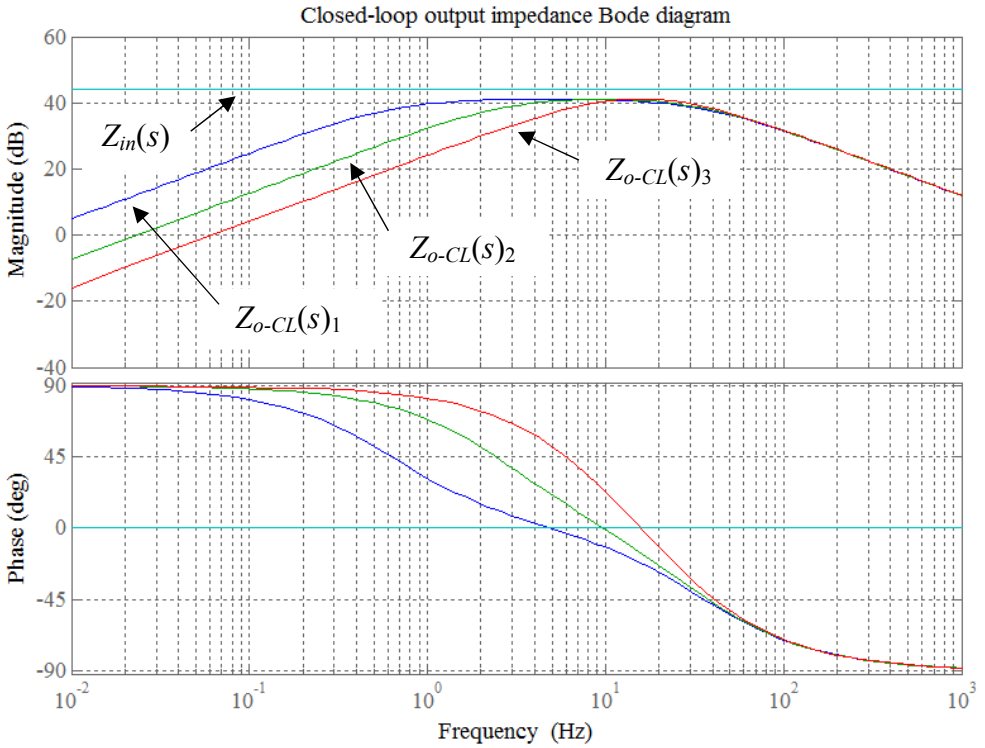


c)

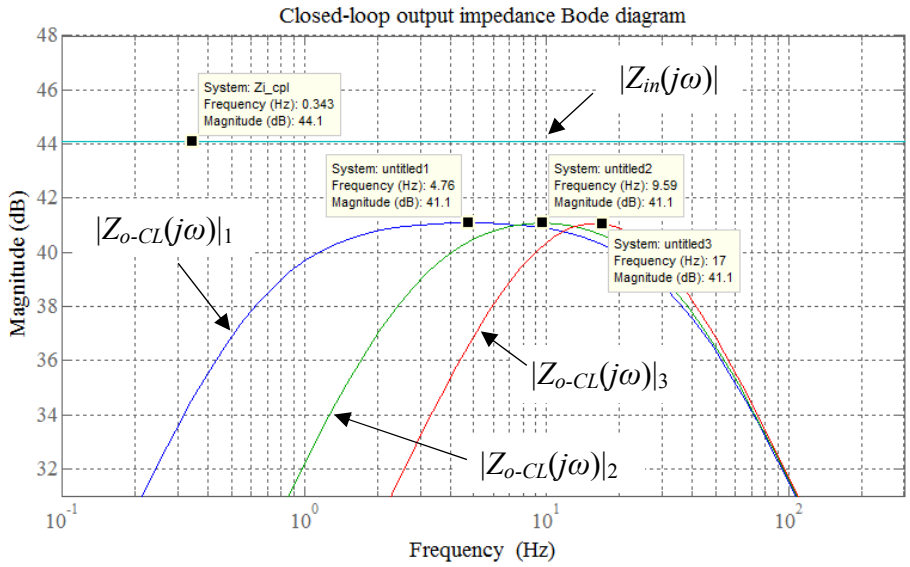


Fig. 6.19. Bode diagram of a) loop gain, b) closed-loop output impedance $Z_{o\text{-}CL,1st}(s)$ and $Z_{in}(s)$, c) detail of the maximum magnitudes. Sub-indexes 1, 2 and 3 stands for f_C 1 Hz, 4 Hz and 10 Hz respectively.

ω_C [rad/s]	$k_{dif,max}$	k_i	k_p	$T(s)$	$Z_{o\text{-}CL,1st}(s)$
2π(1)	2.0008	$72.0\cdot10^{-3}$	$2.7076\cdot10^{-4}$	$T(s)_1$	$Z_{o\text{-}CL}(s)_1$
2π(4)	2.0129	$17.7\cdot10^{-3}$	$1.1\cdot10^{-3}$	$T(s)_2$	$Z_{o\text{-}CL}(s)_2$
2π(10)	2.0778	$6.6\cdot10^{-3}$	$3.0\cdot10^{-3}$	$T(s)_3$	$Z_{o\text{-}CL}(s)_3$

Table 6.5. Design of three different DC-link voltage controllers with the same ΔZ_{dif}.

According to the aforementioned, the final DC-link voltage controller has been designed for f_C=10 Hz and ΔZ_{dif}= 3 dB. Then, taking into account power stage parameters of Table 6.3, DC-link voltage controller parameters are k_i=6.6·10^{-3} and k_p=3.0·10^{-3}. Note that the design is carried out considering the maximum load conditions, so that it is necessary to check that Middlebrook's stability criterion is also fulfilled for the whole range of load conditions, i.e. from P_o=300 W to P_o=1000 W. This is verified by Fig. 6.20, in which it is possible to see that the second stage's input impedance is always higher than first stage's closed-loop output impedance.

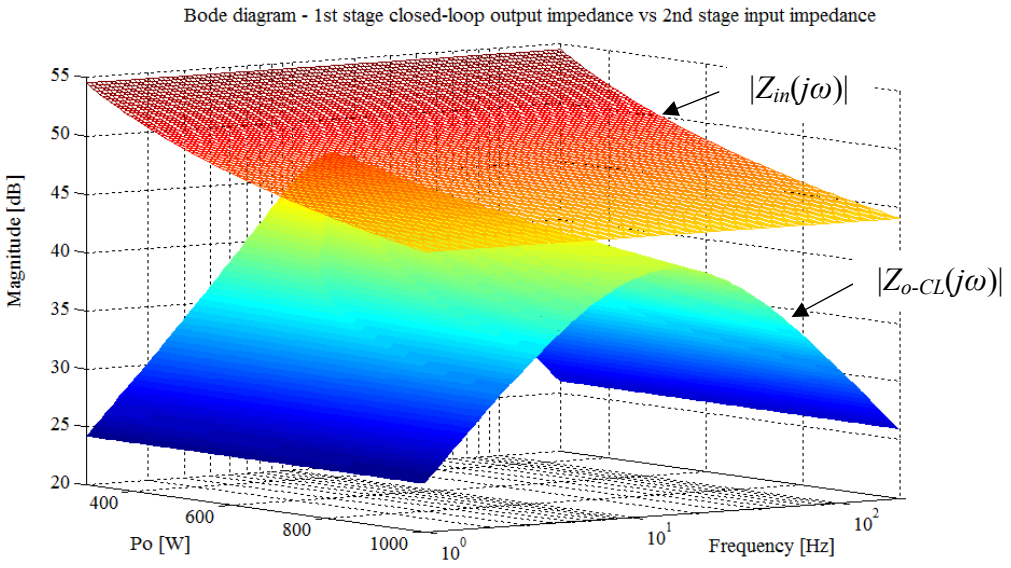


Fig. 6.20. Middlebrook's stability criterion verification of the proposed controller for the load range 300 W – 1 kW.

Finally it is important to remark that the proposed strategy to design the DC-link voltage controller can be applied to any converter independently from the DC-link capacitance as long as the second stage behaves as a constant power sink.

6.3.6 Analogue controller implementation

The proposed PFC controller has been implemented analogically. Three signals need to be sensed from the power stage: $i_{L1}(t)$, $v_{in}(t)$ and $v_C(t)$. As depicted in Fig. 6.21, signals $v_{in}(t)$ and $v_C(t)$ are sensed by means of two voltage dividers while inductor current is sensed by a LA 25-

NP Hall-effect current sensor with 3 turns on the primary side. Hence, sensing signals are defined as follows.

$$v_{in,sens}(t) = k_{Vin} v_{in}(t) = \left(\frac{1}{35}\right) v_{in}(t) \tag{6.99}$$

$$i_{L1,sens}(t) = k_{iL1,sens} i_{L1}(t) = \left(\frac{3}{1000}\right) i_{L1}(t) \tag{6.100}$$

$$v_{C,sens}(t) = k_{Vc} v_C(t) = \left(\frac{5.6}{1005.6}\right) v_C(t) \tag{6.101}$$

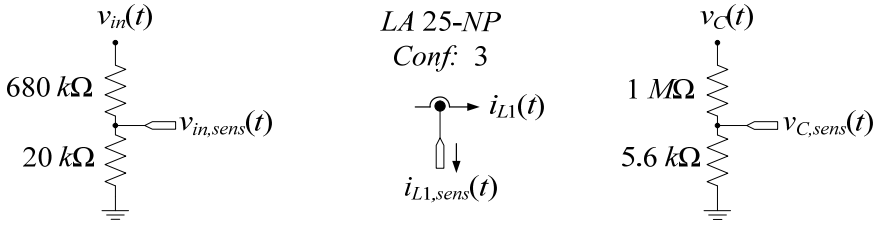


Fig. 6.21. Sensing circuitry of power signals.

The circuit depicted in Fig. 6.22 performs the DC-link voltage regulation. Firstly, voltage error signal $ev_C(t)$ is generated as:

$$ev_C(t) = v_{C,ref}'(t) - v_{C,sens}(t) \tag{6.102}$$

where $v_{C,ref}'(t)$ is the attenuated DC-link voltage reference and it is adjusted externally. Next stage is the PI controller and an output saturation to limit conductance signal $g'(t)$ for safety reasons.

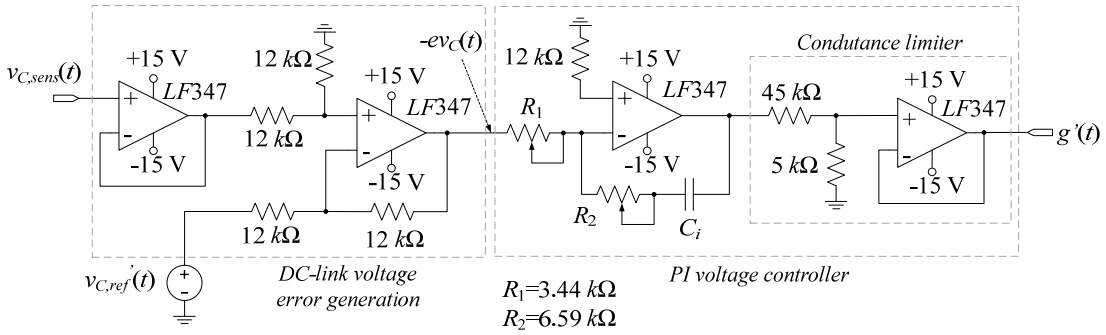


Fig. 6.22. DC-link voltage controller.

Note that transfer function $G_1'(s)$ is defined as

$$G_1'(s) = \frac{G'(s)}{E_{vC}(s)} = \left(\frac{1}{10}\right)\frac{(R_2 C_i s + 1)}{R_1 C_i s} \tag{6.103}$$

If

$$k_{ir} = R_2 C_i \tag{6.104}$$

$$k_{pr} = \frac{1}{10 R_1 C_i} \tag{6.105}$$

it is possible to define $G_1'(s)$ as follows.

$$G_1'(s) = k_{pr} \frac{(k_{ir} s + 1)}{s} \tag{6.106}$$

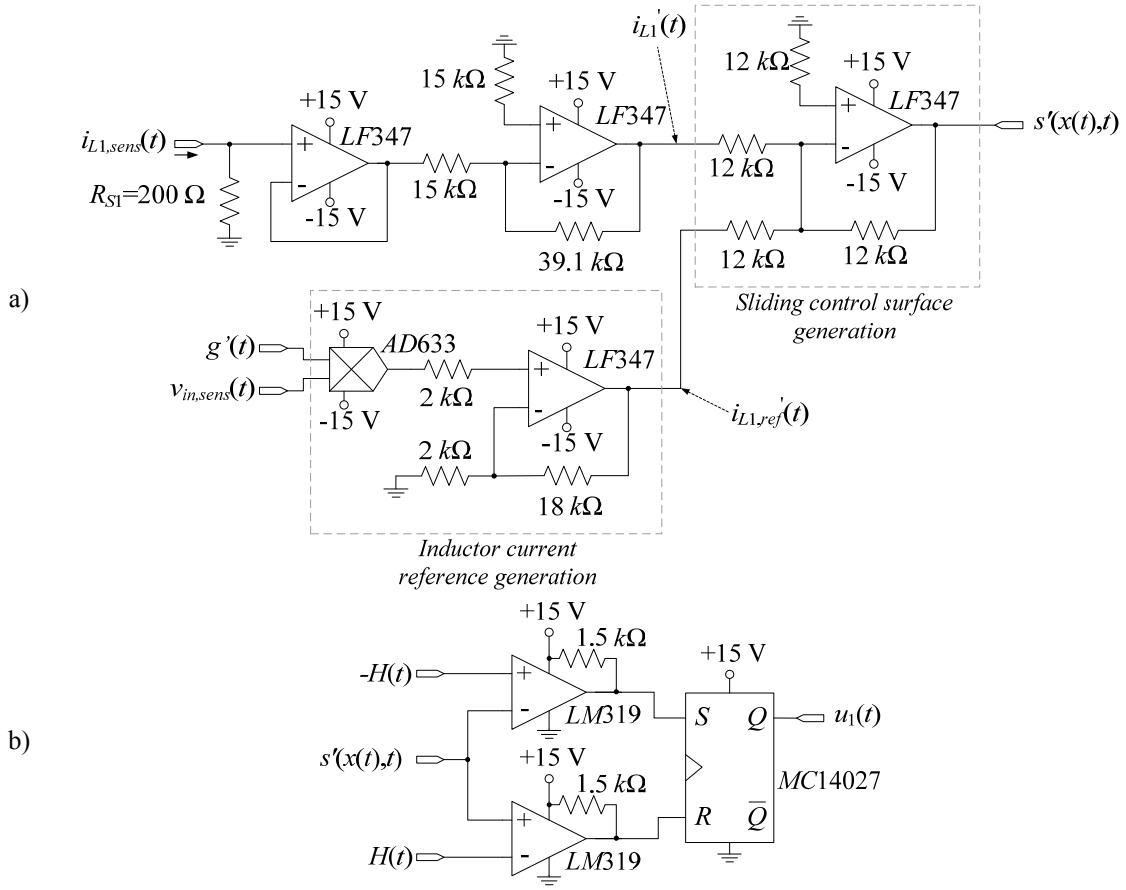


Fig. 6.23. Hysteretic current-mode controller. a) Sliding-mode control surface implementation. b) Control signal generation.

The hysteretic current-mode controller is illustrated in Fig. 6.23. On one hand, inductor current reference $i_{L1,ref}'(t)$ is obtained from multiplying conductance signal $g'(t)$ with $v_{in,sens}(t)$. This operation is carried out by an AD633 multiplier and a non-inverting amplification stage with a gain of 10 that compensates the inherent output attenuation of the aforementioned multiplier. Thus, inductor current reference $i_{L1,ref}'(t)$ comes defined as follows.

$$i_{L1,ref}'(t) = g'(t) v_{in,sens}(t) \tag{6.107}$$

On the other hand, signal $i_{L1}'(t)$ is defined as

$$i_{L1}'(t) = -k_{iL1,gain} i_{L1,sens}(t) = -\left(\frac{200 \cdot 39.1}{15}\right) i_{L1,sens}(t) \tag{6.108}$$

Sliding-mode control surface $s'(x(t),t)$ is given by the negative sum of signals $i_{L1,ref}'(t)$ and $i_{L1}'(t)$, so that

$$s'(x(t),t) = -\left(i_{L1}'(t) + i_{L1,ref}'(t)\right) = k_{iL1,gain} i_{L1,sens}(t) - g'(t) v_{in,sens}(t) \tag{6.109}$$

and it is sent to two LM319 comparators that compare $s'(x(t),t)$ with both hysteresis signals $H(t)$ and $-H(t)$. These comparators are connected to the SET and RESET inputs of a MC14027 flip-flop, which generates signal $u_1(t)$ (see Fig. 6.23.b).

Finally, Fig. 6.24 illustrates the employed circuit for hysteresis modulation. Signal $v_{in}(t)$ is firstly attenuated and amplified next aiming to generate a saturated signal at the output of the saturation block. Then, this signal is attenuated 10 times to reduce the width of the hysteresis to a maximum voltage of 1.2 V approximately. At the end of the hysteresis modulation two diodes are connected so that hysteresis signal $H(t)$ will be the higher signal of both $H_{mod}(t)$ and $H_{min}(t)$. Signal $H_{mod}(t)$ comes from the modulation circuit while $H_{min}(t)$ is introduced externally to ensure a minimum hysteresis voltage level to limit the maximum switching frequency of the system around the zero-crossing area. An inverting circuit is used to generate signal $-H(t)$.

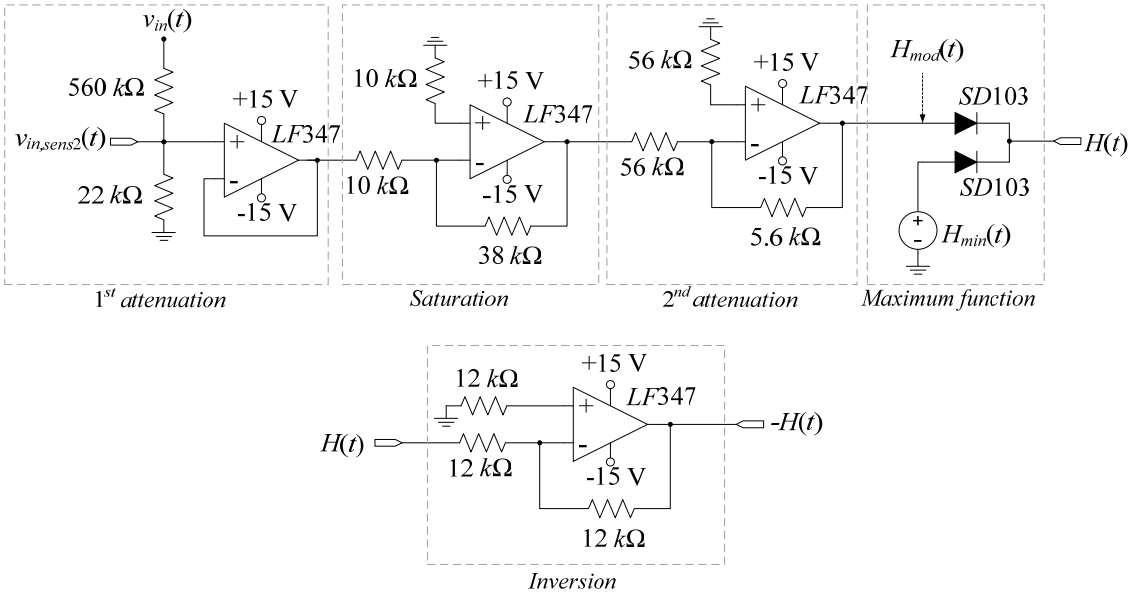


Fig. 6.24. Employed circuit for hysteresis modulation.

The circuit implementation can be modelled by the block diagram that is illustrated in Fig. 6.25.a. Resistors R_1 and R_2 of the PI circuit are calculated through the equivalent block diagram depicted in Fig. 6.25.b where $G_1(s)$ and $G_{GVc}(s)$ can be clearly identified. Note that feedback paths of the equivalent block diagram present an unity gain and sliding control surface is now $s(x(t),t)=i_{L1}(t)-g(t)\cdot v_{in}(t)$ as defined initially. Therefore, it is possible to write:

$$G_1(s)=\left(k_{Vc}k_{Vin}\right)\left(k_{iL1}\right)^{-1}G_1'(s)=\left(k_{Vc}k_{Vin}k_{pr}\right)\left(k_{iL1}\right)^{-1}\left(\frac{k_{ir}s+1}{s}\right) \tag{6.110}$$

where

$$k_{iL1}=k_{iL1,sens}k_{iL1,gain} \tag{6.111}$$

Therefore, DC-link voltage controller design parameters k_i and k_p are defined as

$$k_i=k_{ir} \tag{6.112}$$

$$k_p=\frac{k_{Vc}k_{Vin}k_{pr}}{k_{iL1,sens}k_{iL1,gain}} \tag{6.113}$$

Thus, PI circuit resistors R_1 and R_2 are given by the following expressions.

$$R_2=\frac{k_i}{C_i} \tag{6.114}$$

$$R_1=\frac{k_{Vc}k_{Vin}}{10\left(k_pk_{iL1,sens}k_{iL1,gain}\right)C_i} \tag{6.115}$$

If C_i=1 µF, k_p=3.0·10^{-3} and k_i=6.6·10^{-3}, the value of PI resistors are R_1=3.44 $k\Omega$ and R_2=6.59 $k\Omega$.

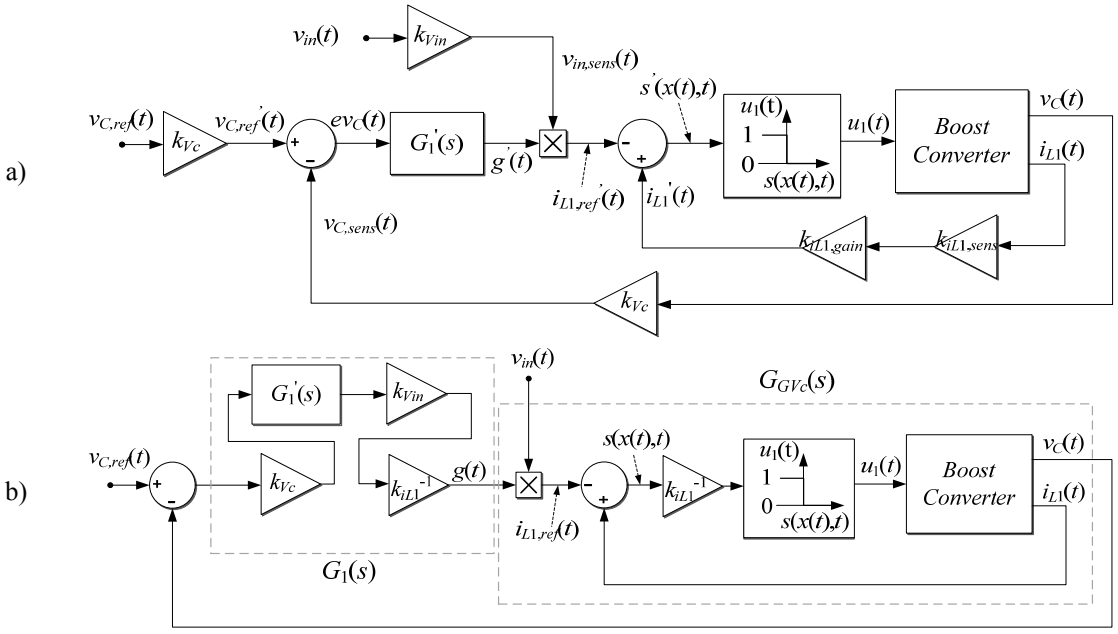


Fig. 6.25. Block diagram of the analogue circuit. a) Implemented circuit. b) Equivalent diagram.

6.3.7 Simulation and experimental results

The pre-regulator has been simulated using the PSIM package and implemented in a modular prototype (see Fig. 6.26) to validate the feasibility of the proposed DC-link capacitor reduction and PFC controller design for a boost converter. A DC-link overvoltage protection has been added for safety reasons. The selected components of the power stage are listed in Table 6.6.

Component	Component Reference	Part # / Value
Diode bridge	*DB*	PB3006
SiC MOSFET	Q_1	CMF1012D
SiC Diode	D_1	IDH10SG60C
Inductor	L_1	77439-A7/ 620 µH
DC-link capacitor	*C*	MKP1848S63070JY5F / 30 µF
		MKP1848S61010JY2B / 10 µF

Table 6.6. Selected components for the power stage prototype.

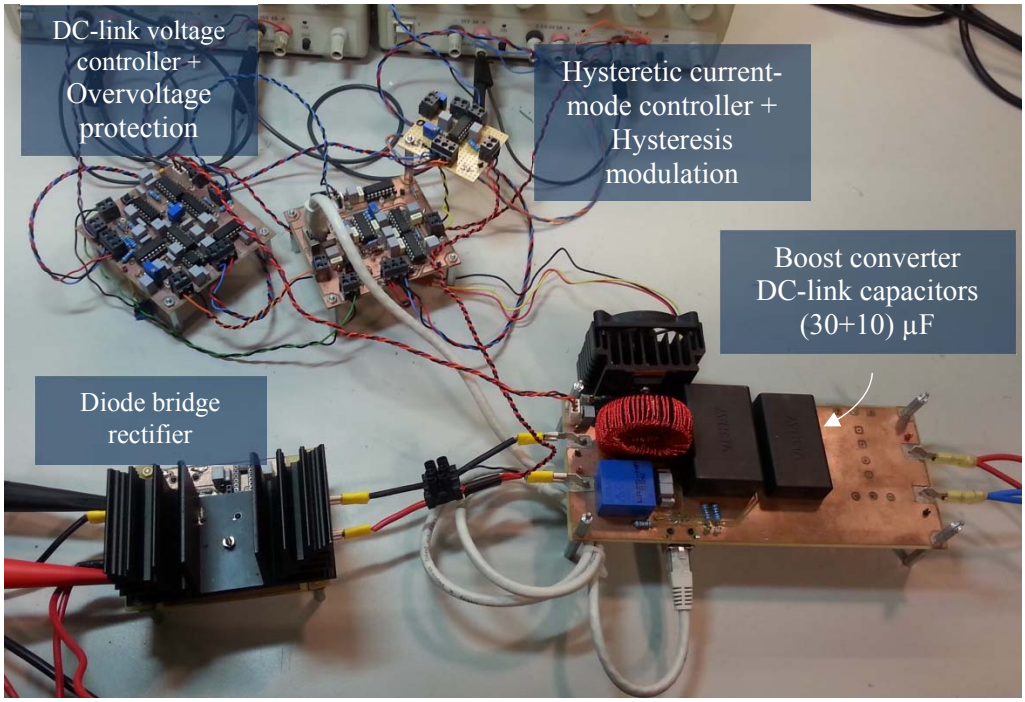


Fig. 6.26. Implemented power converter and analogue controller.

Fig. 6.27 depicts the steady-state response of the system under the nominal power conditions, which are listed in Table 6.7. In particular, Fig. 6.27.a illustrates the PSIM simulation while Fig. 6.27.b illustrates the experimental results. It can be seen in both figures that line voltage $v_{AC}(t)$ and line current $i_{AC}(t)$ are proportional and in phase, so that the achievable power factor is high. The resulting low-frequency harmonics of line current $i_{AC}(t)$ under these conditions are depicted in Fig. 6.28. As it can be seen, the system complies correctly with the IEC 61000-3-2 standard regulation limits for Class A equipment.

Parameter	Symbol	Value
Line voltage	V_{AC}	230 V_{RMS}
Line frequency	f_{AC}	50 Hz
DC-link voltage	V_C	400 V_{DC}
Output power load	P_o	1 kW

Table 6.7. Nominal power conditions.

a)

b)

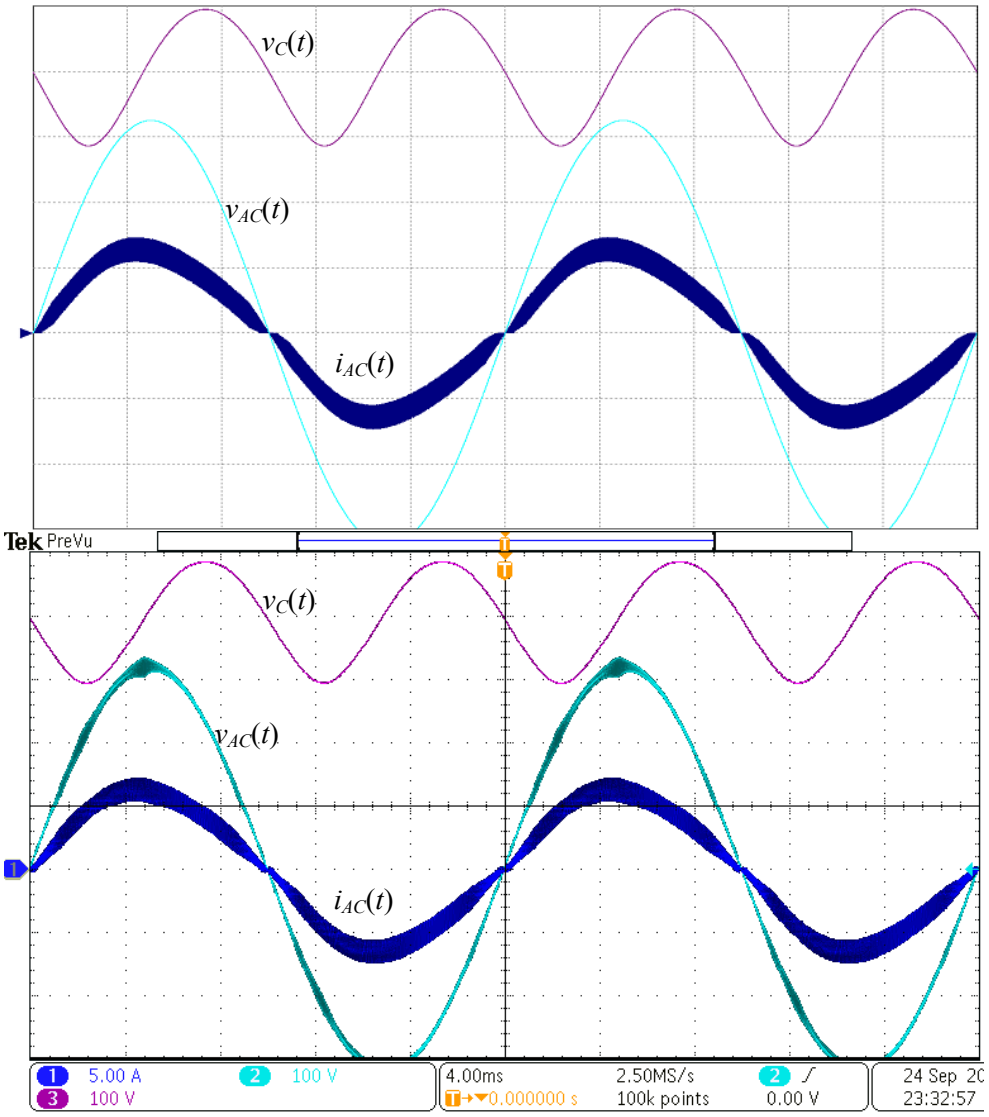


Fig. 6.27. Steady-state response of the pre-regulator (4 ms/div): a) simulation and b) experimental results. CH1: line current $i_{AC}(t)$ (5 A/div). CH2: line voltage $v_{AC}(t)$ (100 V/div). CH3: DC-link capacitor voltage $v_C(t)$ (100 V/div).

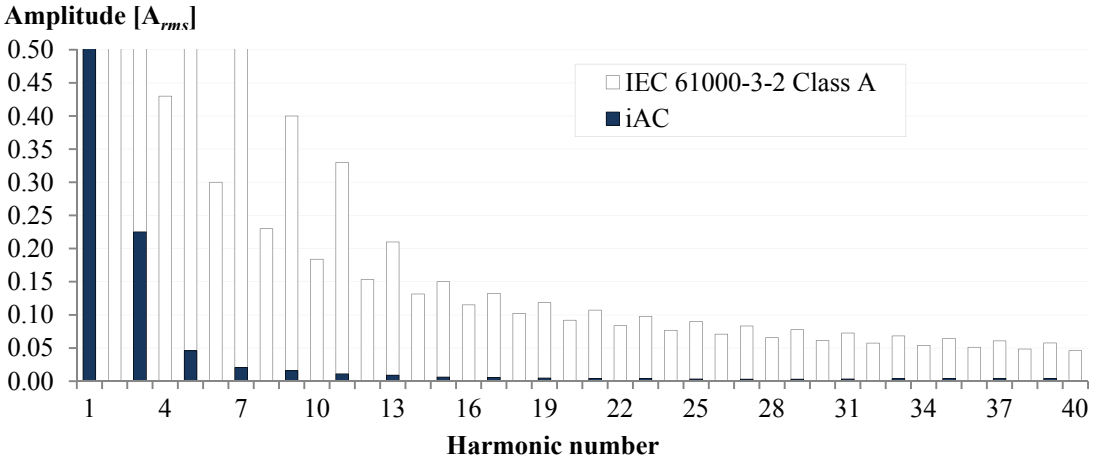
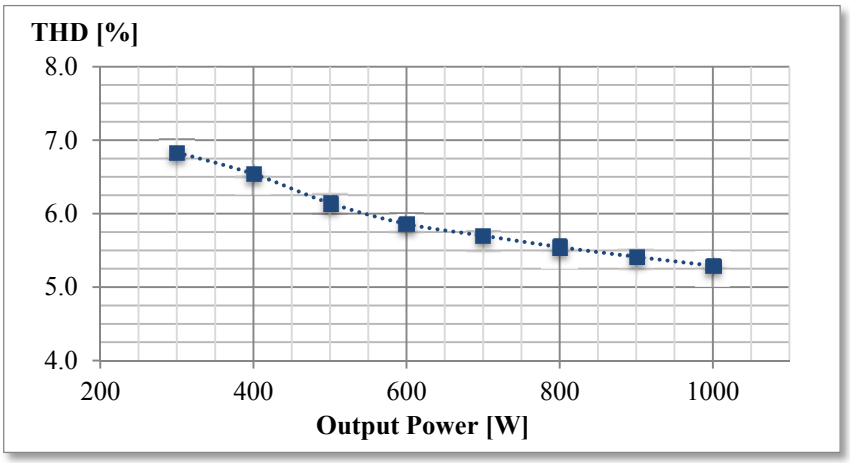


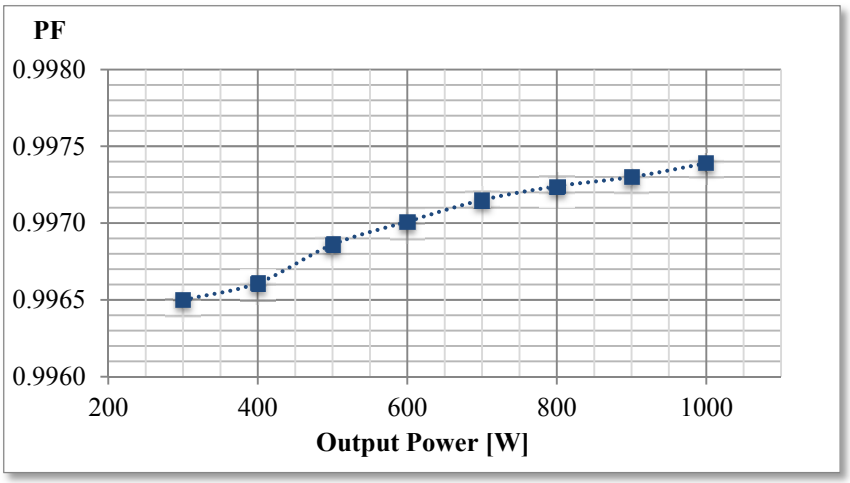
Fig. 6.28. IEC 61000-3-2 Class A harmonic limits and measured low-frequency harmonics of line current $i_{AC}(t)$ under nominal power test conditions.

The THD, PF and efficiency of the prototype, which did not take into account the power consumption of neither the controller nor the driver, were measured with a WT3000 Yokowaga Power Analyzer for different load conditions and a constant DC-link voltage of 400 V_{DC} (see Fig. 6.29). It can be observed that the best results correspond to the maximum load conditions, in which the system exhibits a THD of 5.29 %, a PF of 0.9974 and an efficiency of 97.26 %.

a)



b)



c)

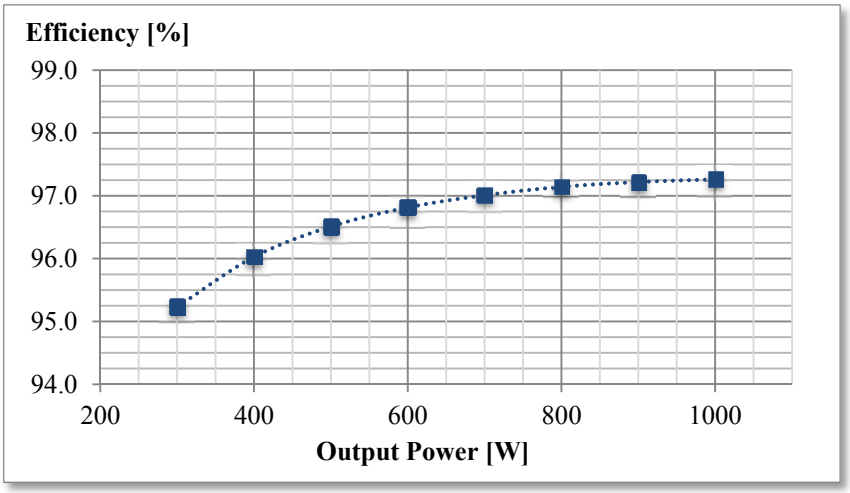


Fig. 6.29. Measured a) total harmonic distortion (THD), b) power factor (PF) and c) efficiency.

a)

b)

c)

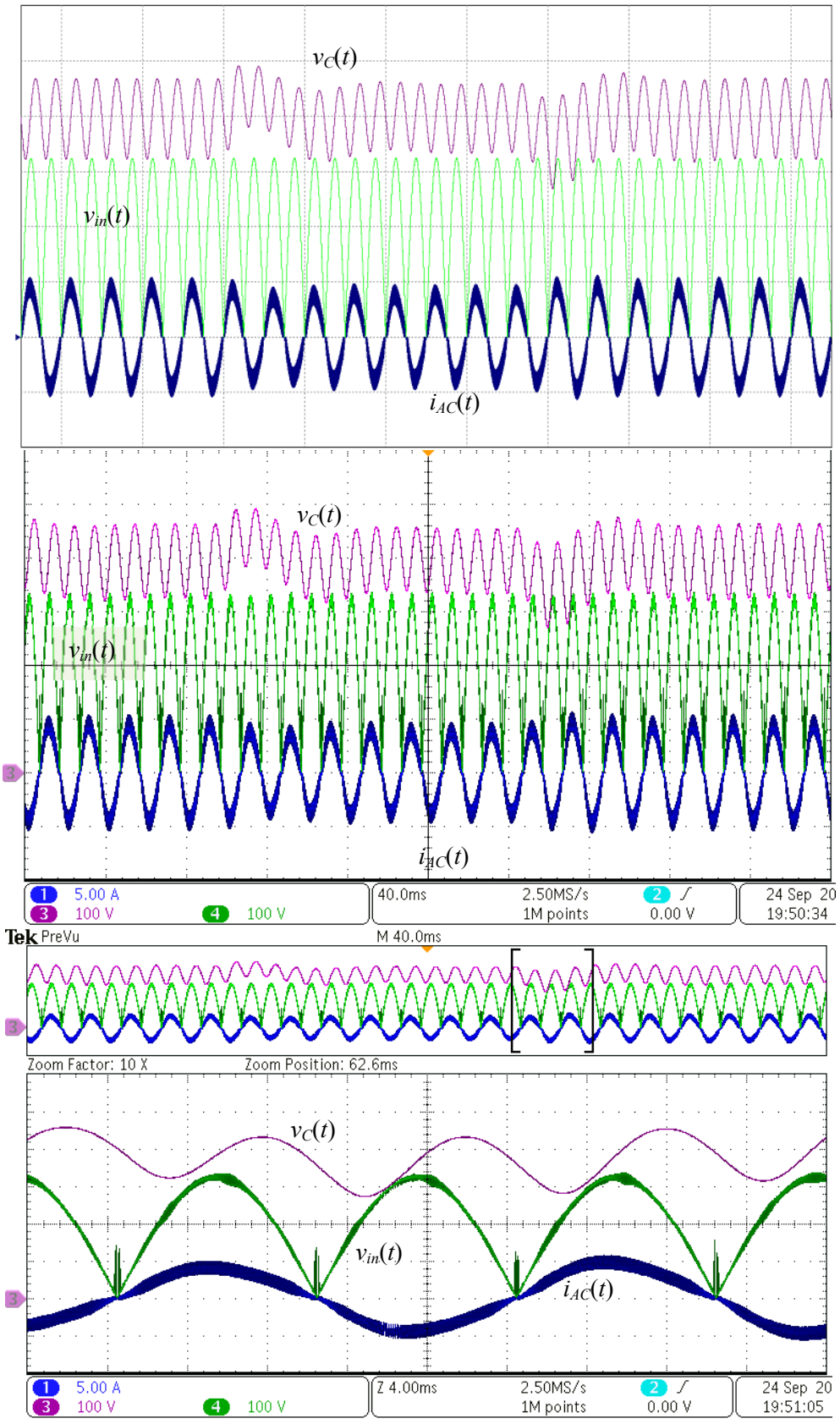


Fig. 6.30. Transient response of the pre-regulator to periodic step output load perturbations of 100 W (100 ms/div): a) simulation and b) experimental results. c) Zoom of transient response to a load step change from 600 W to 700 W (4 ms/div). CH1: $i_{AC}(t)$ (5 A/div). CH3: $v_C(t)$ (100 V/div). CH4: $v_{in}(t)$ (100 V/div).

The transient response of the pre-regulator to periodic step perturbations of the output load from 700 W to 600 W every 150 ms is illustrated in Fig. 6.30. The PSIM simulation is depicted in Fig. 6.30.a while Fig. 6.30.b and Fig. 6.30.c have been experimentally obtained. It can be observed that although the DC-link voltage is regulated at 400 V as desired, the output load step change from 700 W to 600 W produces a transient response with a relatively high voltage peak that almost reaches the level of 500 V. It also worth noting in Fig. 6.30.c how $v_C(t)$ experiments an important approximation to the rectified input voltage $v_{in}(t)$ during the output load step change from 600 W to 700 W. However, Fig. 6.31 demonstrates that the system is not capable to cope with an output load step change from 550 W to 700 W without distorting the AC current line $i_{AC}(t)$ because $v_C(t)$ decreases too much and the sliding-mode regime of $i_{L1}(t)$is lost.

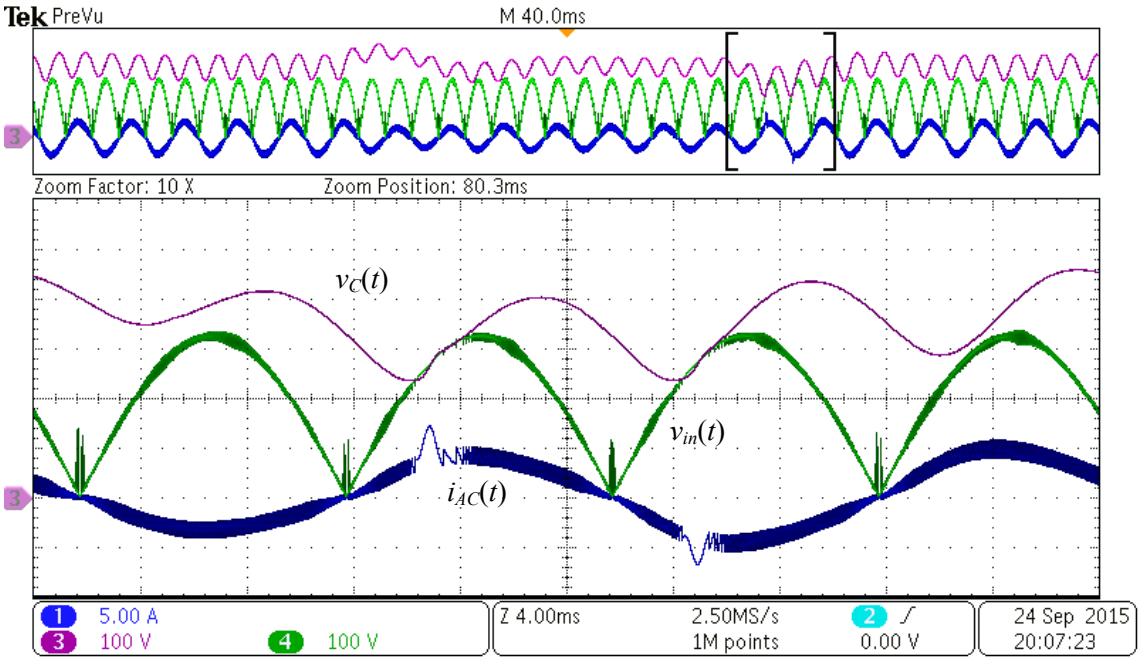


Fig. 6.31. Line current distortion for transient responses from 550 W to 700 W (4 ms/div). CH1: $i_{AC}(t)$ (5 A/div). CH3: $v_C(t)$ (100 V/div). CH4: $v_{in}(t)$ (100 V/div).

6.4 DC-link voltage regulation from the second stage

The second scenario that has been analysed is based on the following considerations:

1. DC-link voltage regulation is performed by the second stage.
2. Output voltage regulation of the second stage is not necessary or the dynamics of this loop can be assumed as constant with respect the rest of the system's dynamics.

These considerations could be used to design a two-stage based battery charger with a highly reduced DC-link capacitance.

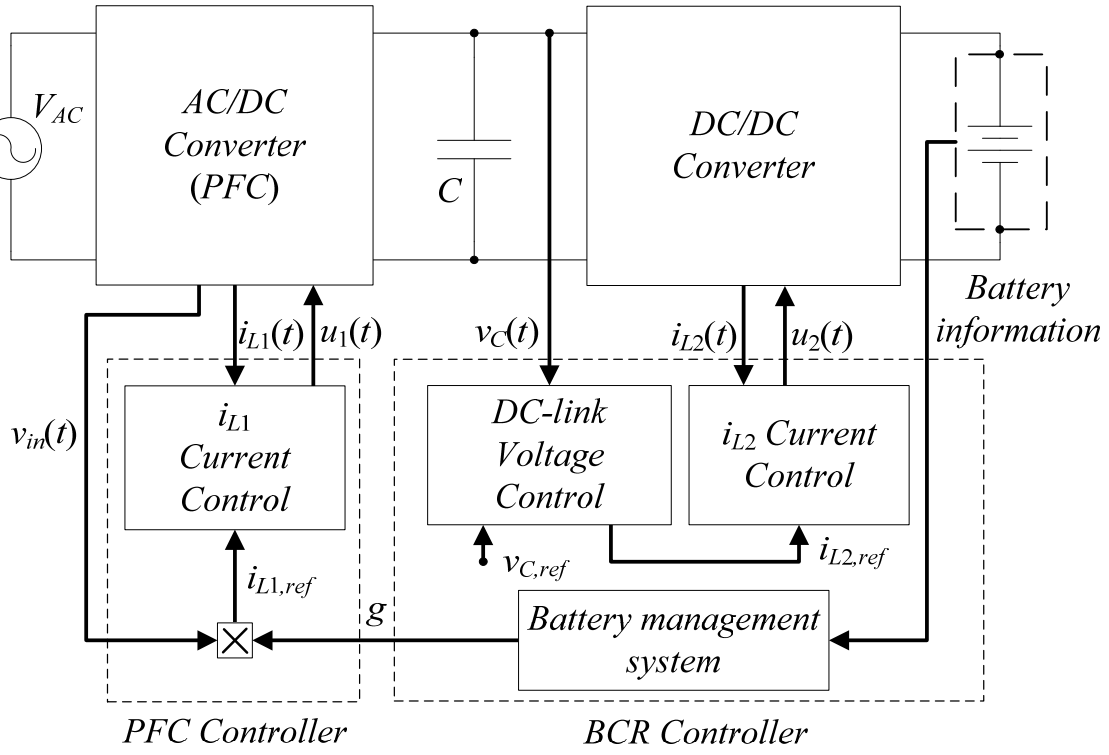


Fig. 6.32. Proposed control design for a two-stage based battery charger with very low DC-link capacitance and DC-link voltage regulation from the second stage.

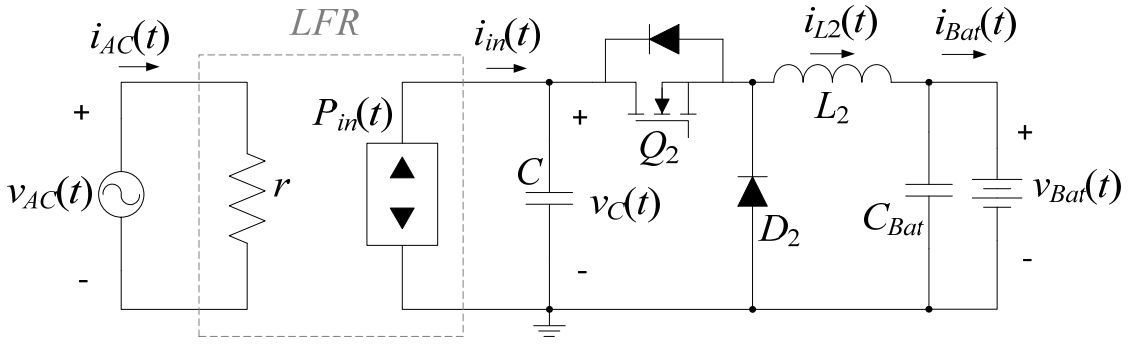


Fig. 6.33. First stage is modelled as an LFR. A buck converter is employed to configure the second stage.

As it can be observed in Fig. 6.32, the DC-link voltage is regulated by the second stage, so that the DC-link voltage controller has to generate the required current reference for the inner loop of the second stage. In this case, the BMS would be the responsible of adjusting the average charging power level by means of conductance $g=r^{-1}$. Remember that this conductance determines the emulated input resistance of the first stage. A noteworthy detail is that $v_{C,ref}$ does not have to be necessarily constant. If a boost converter and a buck converter were selected to configure the first and the second stage of the battery charger respectively (see Fig. 6.33), the DC-link voltage should be always higher than the rectified input voltage and the battery voltage. Therefore, it would be interesting in terms of efficiency inducing a DC-link voltage waveform

as depicted in Fig. 6.34. As it can be observed, the DC-link voltage increases with the rectified input voltage and decreased towards the battery voltage when the rectified input voltage decreases too. Hence, DC-link voltage reference $v_{C,ref}(t)$ could be defined, for example, as

$$v_{C,ref}(t) = V_{C,DC} - V_{C,M}\cos(2\omega_o t) \tag{6.116}$$

where $V_{C,DC}$ is the DC voltage and $V_{C,M}$ is half of the peak-to-peak ripple of $v_{C,ref}(t)$. Although setting the most suitable $V_{C,DC}$ and $V_{C,M}$ is not the aim of this work, they could be adjusted depending on battery voltage V_{Bat}, peak line voltage V_M, etc.

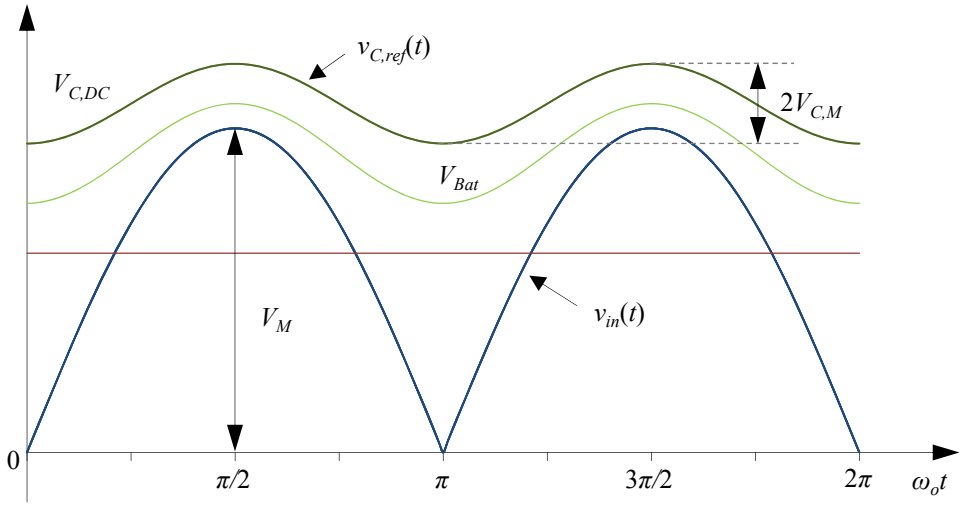


Fig. 6.34. Proposed DC-link voltage waveform.

The principle of this approach is that the DC-link capacitor is storing a very little amount of energy due to its reduced capacitance and, in consequence, almost the whole power that is supplied by the PFC stage is directly transferred to the battery. For that reason, if input power has a square sinusoidal form (assuming that $v_{AC}(t)$ and $i_{AC}(t)$ are both sinusoidal) and the battery voltage is considered constant for one half line cycle, the battery current must exhibit a square sinusoidal form too. This principle is also employed in [122, 123] to reduce the DC-link capacitance. In these works, a square sinusoidal battery current reference is directly generated for the second stage while the DC-link voltage is regulated by the PFC stage. However, regulating the DC-link voltage from the PFC having a very low DC-link capacitance is not recommendable because the PFC controller would not be fast enough to cope with unexpected high load variations. For that reason, this thesis proposes regulating the DC-link voltage from the second stage instead of regulating it from the PFC stage, this ensuring a faster DC-link voltage regulation without distorting the line current.

Hence, it is clear that a very low DC-link capacitance is required to achieve a proper voltage tracking of the DC-link voltage reference depicted in Fig. 6.34. Moreover, it is important to

highlight that, in this case, signals $v_{in}(t)$ and $v_C(t)$ are symmetric from 0 to π/2 rads if the DC-link voltage reference is tracked correctly. Therefore, inductor current ripples would not present the same deformation as in the previous section if fixed frequency current-mode controllers were employed in the PFC stage in this scenario. However, sliding-mode control technique is also applied on the second stage to compare the DC-link voltage controller design with the one designed in the previous section.

Note that in this case, the state vector of second stage is defined as

$$x(t)=\begin{bmatrix} i_{L2}(t) \\ v_C(t) \end{bmatrix} \tag{6.117}$$

Note that C_{Bat} voltage is not considered as a state variable because its voltage is fixed by the battery voltage. Similarly to the boost converter analysis in the previous section, buck converter dynamics can be expressed by means of differential equations (6.34) and (6.35). However, in this case control signal that manages the state of MOSFET Q_2 is $u_2(t)$ while state matrices are defined as follows

$$A_1=\begin{bmatrix} 0 & \frac{1}{L_2} \\ -\frac{1}{C} & 0 \end{bmatrix}, \quad A_2=\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad B_1=B_2=\begin{bmatrix} -\frac{v_{Bat}(t)}{L_2} \\ \frac{i_{in}(t)}{C} \end{bmatrix} \tag{6.118}$$

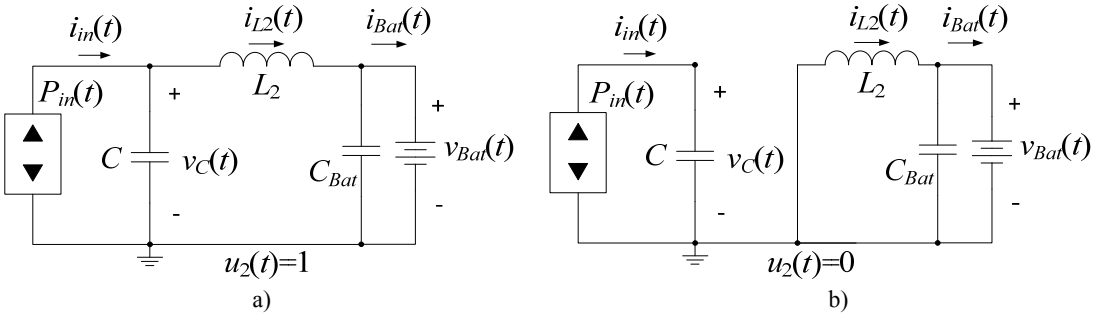


Fig. 6.35. Conduction topologies of a buck converter. a) ON-state. b) OFF-state

Note that an unidirectional buck converter with a power source and one capacitor connected to its input port is the symmetric system of an unidirectional boost converter with a power sink connected to its output capacitor. In consequence, matrices A_1, A_2, B_1 and B_2 of a boost convert are A_2, $-A_1$, $-B_1$ and $-B_2$ of a buck converter respectively. This difference in the sign in some of the matrices lays on the direction of the power flow (including the direction of inductor current $iL_2(t)$) and the definition of the ON state due to the position of the controlled switch.

If sliding-mode control surface $s(x(t),t)$ is chosen as

$$s\left(x(t),t\right)=i_{L2}(t)-i_{L2,ref}(t) \tag{6.119}$$

equivalent control $u_{2,eq}(t)$ results in

$$u_{2,eq}(t)=\frac{L_2\left(\frac{\mathrm{d}\left(i_{L2,ref}(t)\right)}{\mathrm{d}t}\right)+v_{Bat}(t)}{v_C(t)} \tag{6.120}$$

Then, it can be demonstrated that the ideal dynamics of DC-link voltage is given by the following expression

$$\dot{v}_C(t)=-\left(\frac{L_2 i_{L2,ref}(t)}{C v_C(t)}\right)\frac{\mathrm{d}\left(i_{L2,ref}(t)\right)}{\mathrm{d}t}-\frac{i_{L2,ref}(t)v_{Bat}(t)}{C v_C(t)}+\frac{i_{in}(t)}{C} \tag{6.121}$$

Therefore, linearizing around the equilibrium point results in

$$\dot{\tilde{v}}_C(t)\simeq-\frac{V_{Bat}}{CV_C}\tilde{i}_{L2,ref}(t)-\frac{L_2 I_{L2,ref}}{CV_C}\dot{\tilde{i}}_{L2,ref}(t)+\frac{I_{L2,ref}V_{Bat}}{C(V_C)^2}\tilde{v}_C(t)-\frac{I_{L2,ref}}{CV_C}\tilde{v}_{bat}(t)+\frac{\tilde{i}_{in}(t)}{C} \tag{6.122}$$

To obtain current $i_{L2,ref}$ to DC-link voltage transfer function it is necessary to force $\tilde{v}_{Bat}(t)=0$ and $\tilde{i}_{in}(t)=0$ before applying a Laplace transformation on (6.122).

$$G_{iL2refVc}(s)=\frac{\tilde{V}_C(s)}{\tilde{I}_{L2,ref}(s)}=-\left(\frac{I_{L2,ref}L_2}{CV_C}\right)\frac{\left(s+\frac{V_{Bat}}{I_{L2,ref}L_2}\right)}{\left(s-\frac{I_{L2,ref}V_{Bat}}{C(V_C)^2}\right)} \tag{6.123}$$

Note that in this case, the previous transfer function presents an unstable pole located on the right hand side of the *s* plane and one stable high frequency zero, which is the inverse situation than transfer function $G_{GVc}(s)$ in the previous section.

The DC-link voltage controller has been selected with the same form as the previous section.

$$G_1(s)=k_p\frac{(k_i s+1)}{s} \tag{6.124}$$

Parameter	Value
V_{Bat}	300 V
$I_{L2,ref}$	3.33 A
V_C	350 V
C	10 µF
L_2	720 µH
k_p	-4.758
k_i	$89\cdot10^{-3}$

Table 6.8. Design parameters for the DC-link voltage controller with highly reduced capacitance.

Considering the value of parameters listed in Table 6.8, k_p and k_i have been selected so that the cut-off frequency and the phase margin of the system's loop gain are approximately 6 kHz and 106º respectively (see Fig. 6.36).

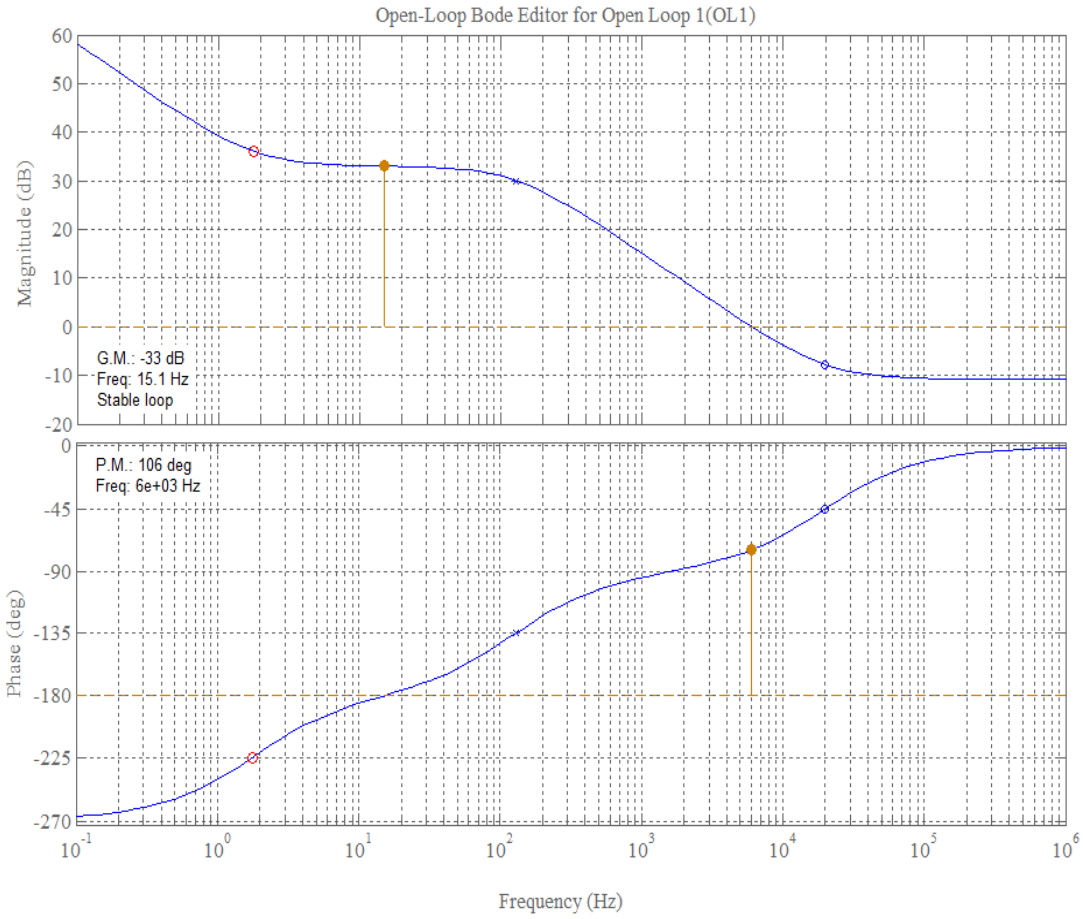


Fig. 6.36. Gain loop frequency response.

Finally, Fig. 6.37 illustrates the simulated steady-state operation of the system for the proposed DC-link capacitance (C=10 µF) and the designed DC-link voltage controller. These simulation results have been carried out also considering two different battery voltage conditions. The rest of simulation parameters can be found in Table 6.9. A hysteretic current-mode controller has been selected to regulate $i_{L2}(t)$ and hysteresis modulation has also been employed to avoid the DCM operation of the buck converter near to the zero crossing area of the line voltage. Conductance g has been defined constant in each simulation because this parameter is meant to vary very slowly according to the SoC of the battery. In addition, the discrete-time SM-based inductor current controller designed in Chapter 4 for the PFC stage cells has been employed here to regulate $i_{L1}(t)$ and demonstrate that the use of fixed-frequency controllers in this case is not an issue.

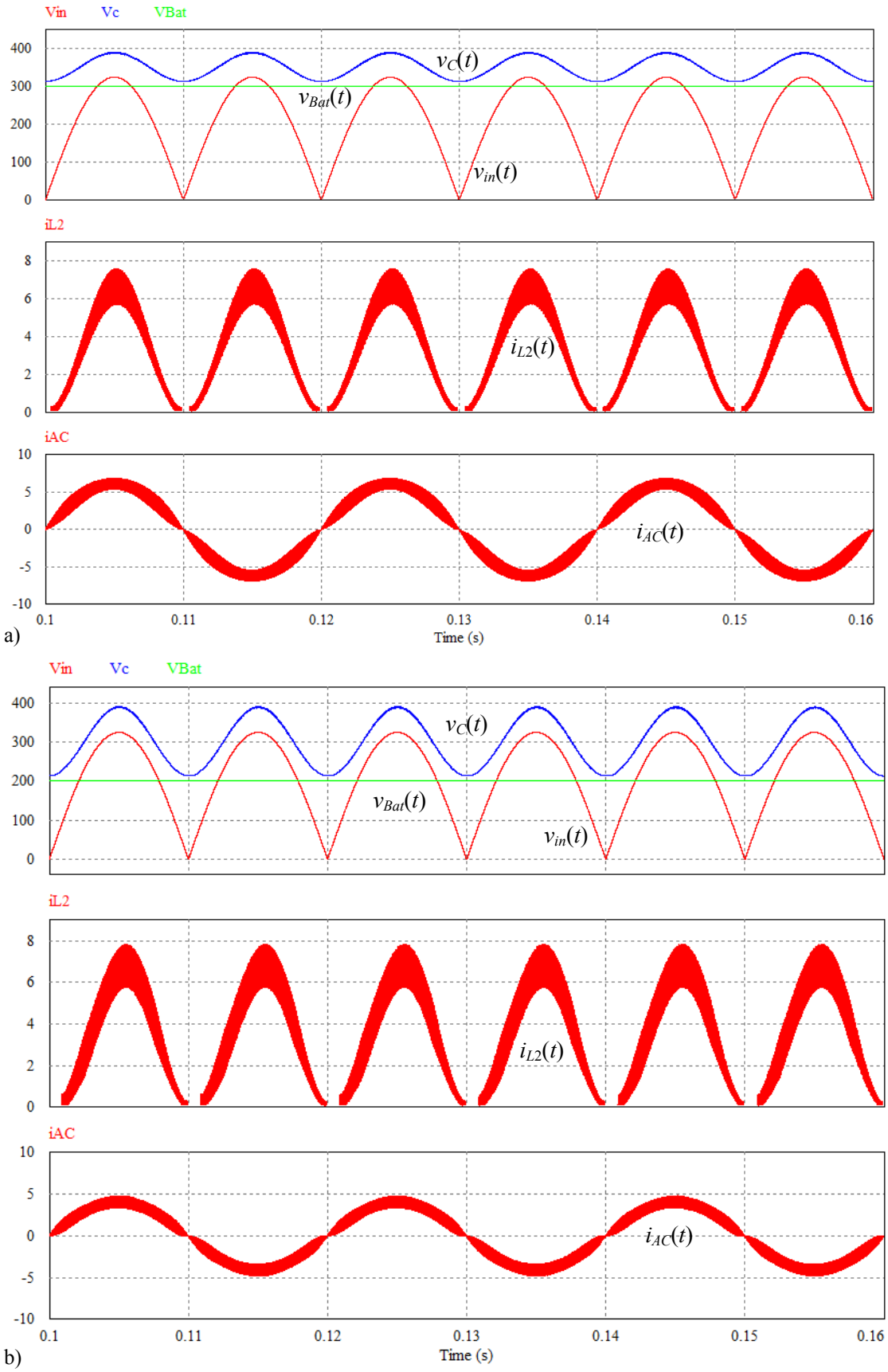


Fig. 6.37. Steady-state simulation with the proposed DC-link voltage controller from the second stage for two different battery voltage conditions. a) Simulation A V_{Bat}=300 V. b) Simulation B V_{Bat}=200 V.

Parameter	Value in simulation A	Value in simulation B
V_{AC}	230 V_{RMS}	
f_{AC}	50 Hz	
L_1	620 µH	
g	18.9 mS	12.6 mS
V_{Bat}	300 V	200 V
$V_{C,DC}$	350 V	300 V
$V_{C,M}$	30 V	80 V
f_{SW} (PFC stage)	60 kHz	

Table 6.9. Simulation parameters for the second DC-link capacitance reduction approach.

It is important to highlight that, despite the very low DC-link capacitance, the first stage behaves as an LFR correctly because current $i_{AC}(t)$ is proportional and in phase with the line voltage $v_{AC}(t)$. DC-link voltage is also properly regulated by the second stage and allows the correct operation of both stages. As expected, $i_{L2}(t)$ exhibits a high variation along a half line cycle since it must ensure the correct DC-link voltage reference tracking. Finally, it is worth commenting that the use of this type of battery charging method is under investigation to determine its consequences on the battery properties [124, 125].

6.5 Conclusions and future work

In this chapter, the reduction of the DC-link capacitance has been analysed in detail for two scenarios. The first one considers that the DC-link voltage is regulated by the first stage and the second stage behaves as a constant power sink. In this case, it is possible to reduce the DC-link capacitance until a minimum value so that the DC-link voltage and the rectified input voltage become tangent. Although, this reduction implies the presence of a high voltage ripple in the DC bus that could eventually affect the performance of the PFC inductor current controller, it has been confirmed that hysteretic current-mode controllers are able to exhibit a good performance. The proposed PFC controller includes an analogue PI controller which has been designed by means of the application of Middlebrook's stability criterion,

The second approach, consisting in a variable DC-link voltage reference tracking, allows a further reduction of the DC-link capacitance. In this case, the DC-link voltage regulation depends on the second stage and the voltage reference can be adjusted, for example, according to the rectified input voltage and the battery voltage. It is important to highlight that this strategy results in a highly variable battery current because the DC-link capacitor is not able to store

much energy. It is expected to validate experimentally the feasibility of the proposed DC-link capacitance reduction and voltage tracking in the future.

Future work regarding the first scenario would include an experimental performance comparison of the proposed hysteretic current-mode controller with respect conventional constant-frequency-based current-mode controllers. It could be also interesting designing an enhanced PFC controller based on a hysteretic current-mode controller whose hysteresis was modulated depending not only on the rectified input voltage but also on the load conditions. In this sense, equation (6.31) could be used to the design a slower control loop that adjusted the DC-link voltage reference depending on the load conditions. Moreover, the DC-link voltage regulation loop could include a Notch filter so that the DC-link voltage controller could be provided with a higher cut-off frequency. It is clear that in this case the use of a Notch filter is of high interest in order to reject oscillations at twice the line frequency produced by the high voltage ripple of the DC bus. The proposed enhanced PFC controller should be implemented in digital controller owing to its expected complexity.

UNIVERSITAT ROVIRA I VIRGILI
DESIGN AND CONTROL OF A BATTERY CHARGER FOR ELECTRIC VEHICLES
Adrià Marcos Pastor

Chapter 7

CONCLUSIONS AND FUTURE WORK

In this thesis the design and control of a 3 kW bidirectional battery charger for plug-in electric vehicles have been presented. It has been demonstrated that it is possible to apply the discrete-time sliding-mode control theory to design constant-frequency-based inductor current digital controllers with fast dynamics. This control design strategy requires the use of a discrete-time model of the controlled variables to derive the corresponding control laws. Although in this particular work, only boost and buck power converters have been analysed, the proposed strategy could be extended to other power converter structures.

The feasibility of the proposed discrete-time sliding-mode-based inductor current controllers has been validated on a fully digitally controlled 3 kW battery charger for plug-in electric vehicles. The proposed battery charger topology consists of a full bridge grid-synchronised rectifier followed by two cascaded stages, which are based on three interleaved cells of 1 kW. The first stage consists of three interleaved boost converters connected in parallel while the second stage is composed by three interleaved buck cells which are connected between the DC-link and the battery.

It has been demonstrated that it is possible to use the derived discrete-time sliding-mode-based inductor current controllers to impose a loss-free resistor behaviour on each cell of the first stage for power factor correction applications. The DC-link voltage regulation loop has been designed by means of a discrete-time PI controller and a Notch filter in order to regulate the DC-link voltage at 400 V_{DC} and achieve a unity power factor. This outer loop is responsible of adjusting the emulated input resistance exhibited by the first stage in order to balance properly the absorbed power from the grid with respect the power delivered to the battery.

Moreover, it has been also verified that it is possible to apply the proposed discrete-time sliding-mode-based controllers on each inductor current of the second stage. A discrete-time PI controller regulates the output voltage by computing the necessary battery current that has to be delivered to the battery. This current reference has been saturated at 8 A in order to force the constant-current operation mode of the battery charger while battery voltage is lower than 380 V. The proper operation of the constant-voltage operation mode has also been validated. The

whole digital controller has been programmed in a single TMS320F28335 DSC from TEXAS INSTRUMENTS.

On the other hand, an important reduction of the DC-link capacitance of battery chargers based on two-cascaded stages has been achieved for two different scenarios by means of a suitable regulation of the DC-link voltage. First analysed scenario considers that the second stage behaves as a constant power load and the DC-link voltage is regulated by the first stage. In this case, a hysteretic current-mode controller has been implemented to regulate the inductor current of the first stage while an analogue PI controller has been employed in the DC-link voltage regulation loop. To ensure the stability of the system, this PI controller has been designed according to Middlebrook's stability criterion. In contrast, the second approach proposes the DC-link voltage regulation from the second stage, this allowing a further reduction of the DC-link capacitance with the expense of inducing high variations on the battery current.

Future research directions derived from this thesis could be focused on the extension of the discrete-time sliding-mode-based digital control design to other power circuit topologies. Other future works could be related to the design of a specific battery management system for testing the implemented battery charger with a real battery. Furthermore, a suitable EMI filter could be designed to comply with the corresponding standards and study stability conditions of the resulting system in both directions of the power flow.

Future works could involve a more deeply analysis of the DC-link capacitance reduction approaches that have been presented in Chapter 6 of this thesis. For example, an enhanced power factor correction controller could be designed as depicted in Fig. 7.1 for those applications in which the second stage behaves as a constant power load. As it can be seen, this controller is based on a hysteretic current-mode controller in which the hysteresis is modulated depending not only on the rectified input voltage, but also on the load conditions. In addition, a slow loop could be introduced to adjust the DC-link voltage reference according to the load conditions. Furthermore, the use of a Notch filter in this application would be high interest since the DC bus exhibits a high voltage ripple. Note that if the PI controller was designed for higher cut-off frequencies and a Notch filter was not employed, the high ripple of the DC-link voltage at twice the line frequency could dramatically increase the amplitude of the third harmonic of line current. On the other hand, DC-link voltage regulation from the second stage is also another future research line that should be explored and tested experimentally. In this sense, both DC-link voltage control strategies for low DC-link capacitance conditions are intended to be experimentally validated on the experimental prototype that is depicted in Fig. 7.2. The power stage of this prototype was designed and implemented in collaboration with the University of Maribor during the pre-doctoral mobility. As it can be observed, the power stage can be

connected to an FPGA-based control board, which has been fully designed at the Faculty of Electrical Engineering and Computer Science, University of Maribor for HYPSTAIR project [126]. It is expected to implement constant and variable frequency-based current-mode controllers and compare the corresponding results.

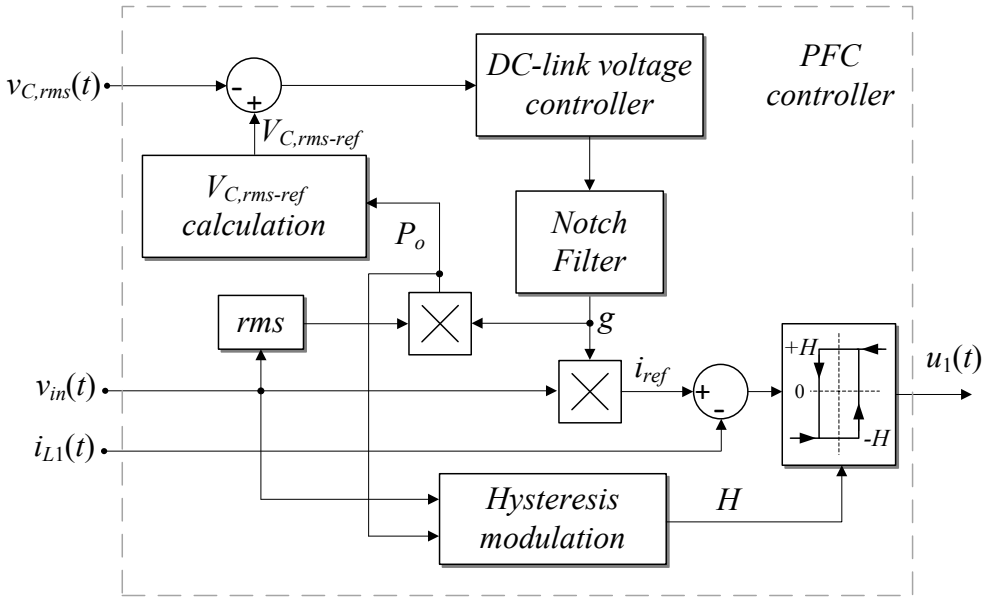


Fig. 7.1. Enhanced PFC controller for low DC-link capacitance conditions.

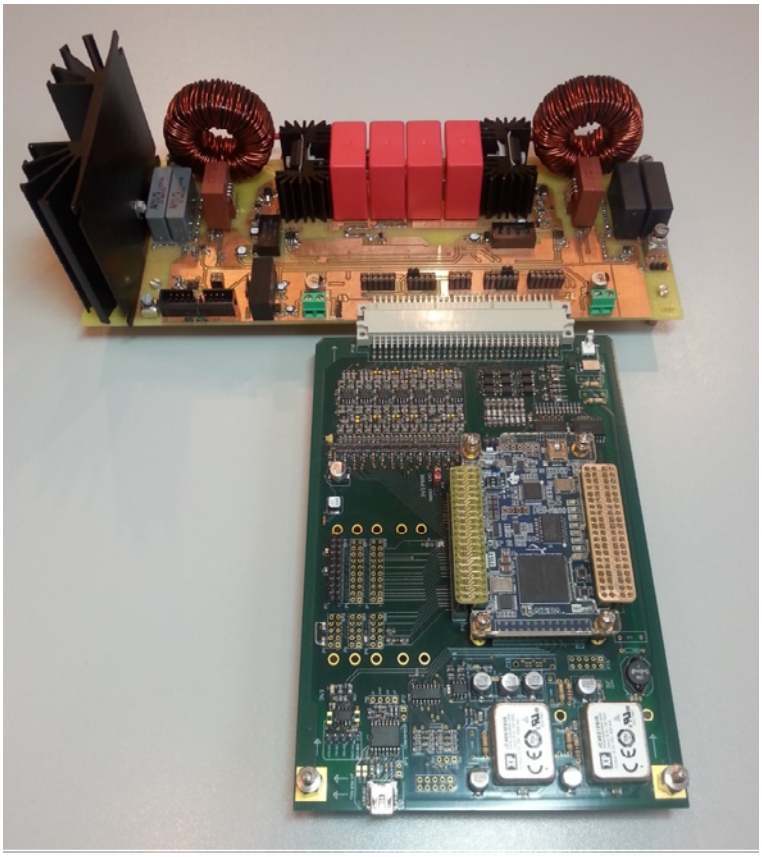


Fig. 7.2. Unidirectional 1 kW battery charger prototype with low DC-link capacitance and FPGA-based control board.

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DESIGN AND CONTROL OF A BATTERY CHARGER FOR ELECTRIC VEHICLES
Adrià Marcos Pastor

Contributions

The main contributions of this doctoral thesis have been published in diverse journals and conferences.

International Journals

[I] E. Vidal-Idiarte, A. Marcos-Pastor, G. Garcia, A. Cid-Pastor, and L. Martinez-Salamero, "Discrete-time sliding-mode based digital PWM control of a boost converter," *IET Power Electronics*, vol. 8, no. 5, pp. 708-714, May 2015.

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